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Optimized QCA SRAM cell and array in nanoscale based on multiplexer with energy and cost analysis

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Abstract. Quantum-dot cellular automata (QCA) has shown great potential in the nanoscale regime as a replacement for CMOS technology. This work presents a specific approach to static random-access memory (SRAM) cell based on 2:1 multiplexer, 4-bit SRAM array, and 32-bit SRAM array in QCA. By utilizing the proposed SRAM array, a single-layer 16×32-bit SRAM with the read/write capability is presented using an optimized signal distribution network (SDN) crossover technique. In the present study, an extremely-optimized 2:1 multiplexer is proposed, which is used to implement an extremely-optimized SRAM cell. The results of simulation show the superiority of the proposed 2:1 multiplexer and SRAM cell. This study also provides a more efficient and accurate method for calculating QCA costs. The proposed extremely-optimized SRAM cell and SRAM arrays are advantageous in terms of complexity, delay, area, and QCA cost parameters in comparison with previous designs in QCA, CMOS, and FinFET technologies. Moreover, compared to previous designs in QCA and FinFET technologies, the proposed structure saves total energy consisting of overall energy consumption, switching energy dissipation, and leakage energy dissipation. The energy and structural analyses of the proposed scheme are performed in QCAPro and QCADesigner 2.0.3 tools. According to the simulation results and comparison with previous high-quality studies based on QCA and FinFET design approaches, the proposed SRAM reduces the overall energy consumption by 25%, occupies 33% smaller area, and requires 15% fewer cells. Moreover, the QCA cost is reduced by 35% compared to outstanding designs in the literature.
Keywords: cost function; energy consumption; majority gate; nanoscale; quantum-dot cellular automata (QCA); Static Random Access Memory (SRAM);

1. Introduction

Quantum-dot cellular automata (QCA) benefits from Coulomb interaction in nanoscale. In this technology, quantum dots are placed at the corners of a square cell, and electrons can occupy these sites by tunneling to them. Because these electrons mutually repulse each other via Coulomb interaction (Tougaw and Lent 1994), so they have to occupy diagonal sites of the square cell. In this case, the electrons can create two states, which are interpreted as '0' and '1' logic values. Multiple QCA cells can be used to devise gates and communication wires using a dedicated clock to control electron mobility and provide the desired Boolean functions (Pudi and Sridharan 2012, Babaie *et al*. 2019). Memory design is a very important area in QCA technology that has attracted a lot of attention. This topic has garnered considerable attention due to the advantages QCA offers in terms of area occupation, frequency, and energy consumption. For a better analysis, this article examines energy consumption in addition to investigating the area, complexity, and delay in QCA-based memory designs. Generally, two types of memory are used in QCA technology: loop-based and line-based memory cells. The loop-based memory structure depends on the storage mechanism using the feedback that includes all four clock zones (Yang *et al*. 2012). The line-based memory structure uses QCA lines to store the previous values (Vankamamidi *et al*. 2005).

In Ref. (Shamsabadi *et al*. 2009), a D-type flip flop scheme is proposed in QCA and the design and simulation of D-type flip flops are presented based on multiplexers. This reference discusses the area, complexity, and delay of the circuit. However, the energy consumption of the flip-flops has not been evaluated. In (Dehkordi *et al*. 2011), a RAM cell in QCA is presented. Moreover, Hashemi and Navi (2012), a novel design is presented for D flip-flops in QCA. These references focus on area, complexity, and delay of memory cells, but not on their energy consumption and QCA cost. In (Angizi *et al*. 2015, Khosroshahy *et al*. 2017), a new majority gate is designed in QCA, and the RAM cells are arranged based on majority gates. The design and simulation of QCA RAM cells are based on the new QCA gates. In (Angizi *et al*. 2015), the area, complexity, and delay of memory cells are reduced using new gates, while energy consumption is not considered. However, in (Khosroshahy *et al*. 2017), besides considering area, cell complexity, and delay, the amount of energy consumption and QCA cost of the presented memory cell are discussed. In (Kianpour and Sabbaghi-Nadooshan 2016), an SRAM memory cell was designed using standard QCA gates. Moreover, the design and simulation of SRAM memory cells and SRAM cell arrays are presented in QCA.

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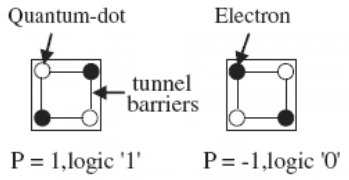
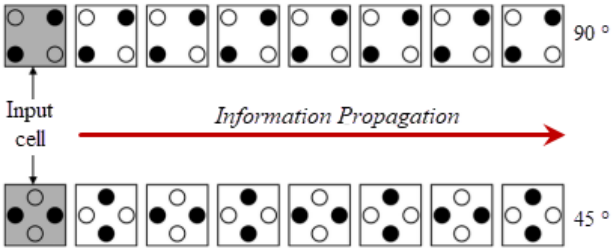
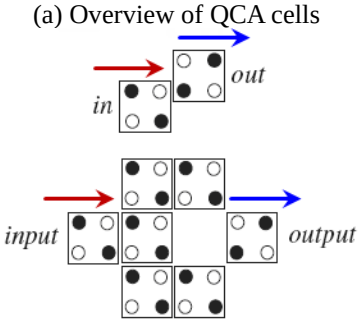


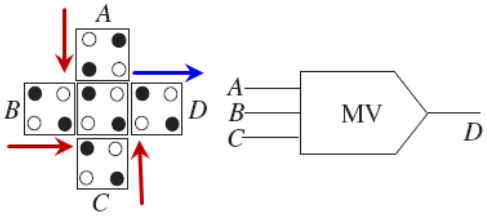
(a) Overview of QCA cells



(b) QCA wire use of 90 ° and 45 ° cells

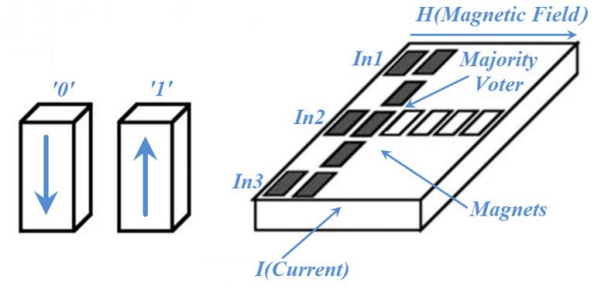


(c) QCA inverter gate

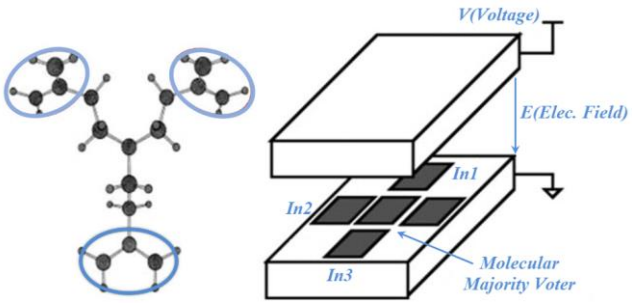


(d) QCA majority gate

Fig. 1 QCA cells, wires, and gates



(a) QCA majority gate in single-domain nanomagnet structure (Vacca *et al*. 2011)



(b) QCA cell and QCA majority gate in molecular structure (Pulimeno *et al*. 2012)

Fig. 2 QCA cell and QCA majority gate

In this reference, achieving the smallest complexity, delay, and area, in comparison with previous designs, is discussed and a comparison is made with transistor-based SRAM cells.

In (Song *et al*. 2020), a RAM cell is proposed using a new 2:1 multiplexer based on a loop with a set/reset line. The efficiency of design is optimized compared to prior structures, but the energy consumption is not considered. Moreover, in this reference, an array of RAM cells is presented in a multilayer QCA structure. The model used in Refs. (Shamsabadi *et al*. 2009, Dehkordi *et al*. 2011, Hashemi and Navi 2012, Angizi *et al*. 2015, Khosroshahy *et al*. 2017, Kianpour and Sabbaghi-Nadooshan 2016 and Song *et al*. 2020) utilizes a loop-based memory structure.

In the present study, we propose an extremely-optimized 2:1 multiplexer, an extremely-optimized MUX-based SRAM cell, and 4-bit/32-bit SRAM arrays. By utilizing the proposed SRAM array, a single-layer 16×32-bit SRAM is presented using an optimized signal distribution network (SDN) crossover technique with read/write capability. The proposed schemes have many advantages over previous designs, such as single-layer structure, low energy consumption, fewer cells, lower QCA cost, and smaller area. Moreover, a comparison is made in terms of complexity, area, delay, energy consumption, and QCA cost with previous designs in CMOS and FinFET technologies.

The remainder of the article is divided into five sections: A review of the basic concepts of QCA is given in Section II. Section III presents a new loop-based SRAM cell and the simulation of energy consumption of the proposed SRAM cell is performed in this section. In Section IV, the SRAM cell array is presented in QCA. Section V presents the results of simulations and discussion. The conclusion is finally given in Section VI.

2. QCA Background: Review of QCA

As field-based nanotechnology, QCA can perform computations in a fundamentally different way. The information is stored by cell polarization, which can be propagated to neighboring cells based on Coulomb

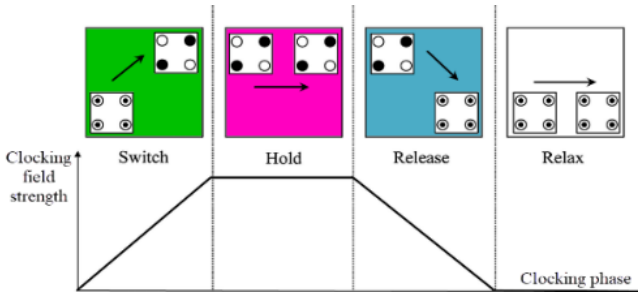


Fig. 3 Clocking mechanism in QCA

interactions. Fig. 1(a) shows the basic cell of the QCA. QCA cells are considered as squares, each consisting of four quantum dots at each vertex, with a pair of electrons placed inside the quantum dots (Chuan *et al*. 2021, Sergeyev 2021). The electrons are established diagonally in the diameter of the cell, which is due to the Coulombic interaction of the electrons at the quantum dots of each cell. Figure 1(a) shows that a cell can be in one of two states of stable energy (referred to as cell polarization) P = +1 and P = -1. Binary information can be encoded based on P = -1 and P = +1 as logic values '0' and '1', respectively.

The QCA basic cells are used in QCA binary wires to transmit a logical input in the cell array to the output cell based on the Coulomb interactions through the cell array. This can be done in two ways, i.e., by using either 90-degree cells or 45-degree cells. The two corresponding QCA wires are shown in Fig. 1(b). A QCA inverter gate is illustrated in Fig. 1(c) in which a polarization injected into the input cell is inverted at the output of the inverter. Fig. 1(d) illustrates the QCA majority gate. A QCA majority gate with three inputs includes five QCA cells. Besides the three inputs, there is a voter cell and an output cell. Eq. (1) describes the three-input majority gate function:

$$M(A,B,C)=AB+BC+AC \tag{1}$$

In two-input QCA-based OR and AND gates, one input of the three-input majority gates is fixed in the value of '1' or '0', respectively.

QCA structures can be implemented using a variety of materials such as metals (Orlov *et al*. 1997), semi-conductors (Smith *et al*. 2003, Chuan *et al*. 2022 and Chuan *et al*. 2020), nanomagnets (Vacca *et al*. 2011), and molecules (Pulimeno *et al*. 2012). Metal QCA structures can be developed on silicon wafers. Nanomagnetic QCA structures are made of magnets. Semiconductor QCA structures can be implemented using electron beam machining lithography on heterostructures such as GaAs/AlGaAs (Perez-Martineza *et al*. 2007). Fig. 2(a) shows the majority gate based on single-domain nanomagnets and nanomagnet QCA structures; additionally, Fig. 2(b) shows molecular QCA structures and the majority gate based on molecular QCA structures.

2.1 QCA Clocking

Four external clock signals in QCA circuits are needed to provide energy to QCA cells and control the data flow (Pourreza *et al*. 2021). These four zones of the external clock are set the QCA cells operative polarization with controls potential barrier's energy among the neighbor quantum dots in QCA cells (Campos *et al*. 2016). Each of these four clock zones in a QCA circuit has a 90-degree difference of phase with its subsequent and earlier clock zones. Fig. 3 is shown the QCA clock zones that can control data propagation through QCA cells. As shown in Fig. 3, each clock zones are indicated with a unique color in the QCA circuit layout.

2.2 Energy consumption model in QCA

Initially, a formulation of cellular automaton power consumption of quantum dots has been developed in (Timler and Lent 2002). Using the Hamiltonian matrix, the energy of a QCA cell or the total energy of the system can be calculated. Hamiltonian can be used for evaluating energy consumption in a set of QCA cells by utilizing the Hartree-Fock approximation and assessing the Coulomb interaction among the cells based on the mean-field approach (Timler and Lent 2002 and Liu *et al*. 2012).

The two main properties of an individual QCA cell in a circuit are the probability of polarization of the static state (which determines the error) and the loss of power under the non-adiabatic clock switching. If a QCA system fails to reach the ground state, it may be incorrect. The probable error of the model presented in (Bhanja and Sarkar 2006) is used to estimate the error in the QCA circuit. The Hamiltonian cell can be used to derive the steady-state polarization of a QCA cell using the Hartree approximation. Hamilton's expression is indicated in Eq. (2).

$$H=\begin{bmatrix} -\frac{1}{2}\sum_i E_k P_i f_i & -\gamma \\ -\gamma & \frac{1}{2}\sum_i E_k P_i f_i \end{bmatrix}=\begin{bmatrix} -\frac{1}{2}E_k\bar{P} & -\gamma \\ -\gamma & \frac{1}{2}E_k\bar{P} \end{bmatrix} \tag{2}$$

where some cells are in the same neighborhood. E_k is the "Kink Energy" or the energy cost of two neighboring cells that have contrary poles. f_i is a geometric characteristic collecting electrostatic deflection with the interval between cells. This energy is dependent on the energy cost of two QCA cells (i and j) with opposite poles and can be calculated in the form of Eq. (3).

$$E_{i,j}=\frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{|r_{i,n}-r_{j,m}|} \tag{3}$$

The polarization of the ith cell is P_i. Also, γ is the tunneling energy between two cellular states controlled by the clock function. Labeling can be simplified by $\bar{P}$ to determine the total polarization weight $\Sigma_i P_i f_i$. Steady-state polarization based on Hamiltonian is obtained as follows:

$$P^{ss}=-\lambda_3^{ss}=\rho_{11}^{ss}-\rho_{00}^{ss}=\frac{E_k\bar{P}}{\sqrt{E_k^2\bar{P}^2+4\gamma^2}}tanh\left(\frac{\sqrt{E_k^2\bar{P}^2+4\gamma^2}}{kT}\right) \tag{4}$$

From Eq. (5):

$$P^{ss}=\frac{E}{\Omega}\tanh(\Delta) \tag{5}$$

where $E = 0.5\ \Sigma_i\ E_k P_i\ f_i$ is the overall kink energy, $\Omega = \sqrt{E_k^2 \bar{P}^2/4 + \gamma^2}$ is the Rabi frequency, and $\Delta = \frac{\Omega}{kT}$ represents the corresponding thermal ratio. Equation (5) is used to measure the probability of observing the system in either of the two modes. Obviously, $P(X = 1) = \rho_{11}^{ss} = 0.5(1 + P^{ss})$ and $P(X = 0) = \rho_{00}^{ss} = 0.5(1 - P^{ss})$. Note that $\rho_{00}^{ss} + \rho_{11}^{ss} = 1$, where ρ_{11}^{ss} and ρ_{00}^{ss} are the probability of observing the QCA cell in Mode 1 or Mode 0.

3. Designing SRAM cell in QCA

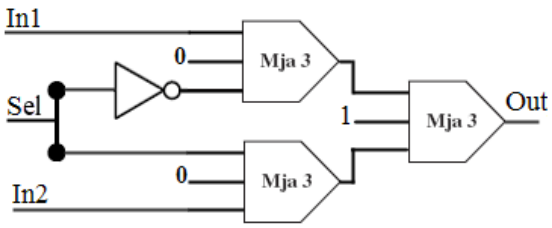
3.1 Designing an optimized 2:1 multiplexer in QCA

The extremely-optimized 2:1 multiplexer presented in this work is implemented using three majority gates, which are also implemented as two-input OR and AND gates with one fixed input. Generally, in using a multiplexer, one of multiple inputs can be selected and directed to the output. Conventional gates are used to implement a 2:1 multiplexer in QCA (see Fig. 4(a)). Thirteen cells, which are used in the proposed 2:1 multiplexer, occupy an area of 0.0096 μm^2. The layout of the proposed QCA-based 2:1 multiplexer is shown in Fig. 4(b). As this figure shows, the delay is 2/4 clock cycles (two phases).

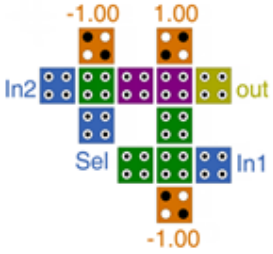
To determine the power dissipation of the proposed extremely-optimized 2:1 multiplexer, we employ QCAPro (Srivastava *et al.* 2011) as an appropriate tool. We study three different tunneling energy levels (0.5, 1, and 1.5 E_k) in the proposed design. Fig. 5 shows the dissipation map of the proposed 2:1 multiplexer at 0.5 E_k. High-energy cells are shown with darker spots. The overall energy dissipation of the presented SRAM bit cell is presented in Table 1. In this table, the energy dissipation is categorized into switching and leakage energies.

3.2 Designing an optimized MUX-based SRAM cell in QCA

The design of SRAM cells is one of the most critical issues in the QCA technology. In general, there are two common types of memory design in QCA (loop- and line-based types) (Vankamamidi *et al.* 2005). The loop-based memory structure uses feedback from the multiplexer output and includes the four clock zones. In this paper, the proposed QCA-based SRAM cell uses the MUX-based memory approach and a transistor-based SRAM bit cell model. This SRAM cell has four control lines and one output as follows: WWL (Write Word-Line), WBL (Write Bit-Line), RWL (Read Word-Line), EN (Enable), and LBL (Local Bit-Line). The proposed SRAM operation principle is given in Table 2. When the values of EN and WWL are "1", the write operation starts and the WBL data is transferred to the memory loop, and then the write operation is completed. Furthermore, the read operation is performed by setting the EN and RWL signals to "1". The SRAM cell schematic is shown in Fig 6(a). The structure presented in this paper makes it possible to use this extremely-optimized MUX-based SRAM cell in the array and access each memory cell alone through the EN line. The layout of the



(a) A 2:1 multiplexer in QCA



(b) the suggested optimized 2:1 multiplexer layout in QCA

Fig. 4 2:1 multiplexer in QCA

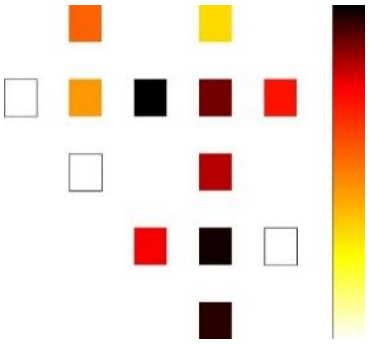


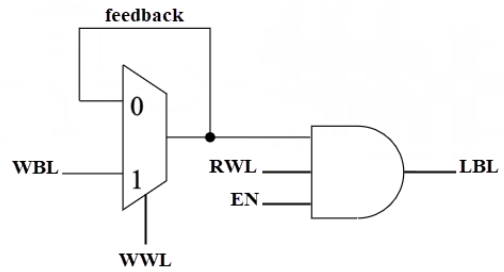
Fig. 5 Energy dissipation thermal map for the suggested optimized 2:1 multiplexer in QCA for 0.5 Ek

Table 1 Energy dissipation of the suggested optimized 2:1 multiplexer

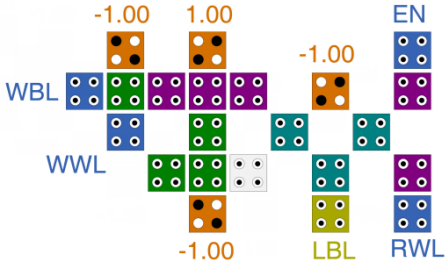
Mode	0.5 E_k	1 E_k	1.5 E_k
Average leakage energy dissipation (meV)	3.59	10.28	17.87
Average switching energy dissipation (meV)	6.03	4.89	3.16
Total energy consumption (meV)	9.62	15.17	21.03

proposed SRAM cell with the new structure based on multiplexer is illustrated in Fig 6(b). The proposed extremely-optimized MUX-based SRAM contains 22 cells covering an area of 0.0174 μm^2 and a maximum delay of 1 clock cycle. In this SRAM cell design, all the layout and timing design rules (Liu *et al.* 2011, 2010) have been observed, so an optimal SRAM cell design is obtained by following the design rules of QCA.

To determine the energy dissipation of the presented structure, we employ QCAPro (Srivastava *et al.* 2011) as an accepted tool. We study three different tunneling energy levels (0.5, 1, and 1.5 E_k) at a temperature of 2 K. The dissipation map of the presented SRAM bit cells at 0.5 E_k is shown in Fig. 7. It is apparently destroyed cells with a high-energy appearance using darker hot spots. From Table 3, the



(a) MUX-based SRAM cell with EN line implementation in QCA



(b) the layout of the proposed optimized MUX-based SRAM cell in QCA

Fig. 6 MUX-based SRAM cell with EN line in QCA

Table 2 The operation of the proposed optimized MUX-based SRAM bit cell

Mode	EN	WWL	WBL	RWL	Memory Loop	LBL
Write	1	1	0	X	0 (next cycle)	Don't care
Write	1	1	1	X	1 (next cycle)	Don't care
Read	1	0	X	0	Unchanged	0
Read	1	0	X	1	Unchanged	Read Value
disable	0	X	X	X	X	X

overall dissipation of the presented SRAM bit cell is categorized into switching and leakage energies.

In Fig. 7, intermediate or voter cells in the presented SRAM consume more energy compared to other cells. Less energy is dedicated to the voter cells in this configuration. The proposed SRAM bit cell shows a significant energy performance compared to other designs.

3.3 Cost function in QCA

In the evaluation and comparison of QCA circuits, the QCA cost can be regarded as a figure of merit (FOM) (Liu *et al*. 2014, Heydari *et al*. 2019). In (Mead and Rem 1979), a cost function is presented based on area-time for finding the most efficient memory design in very-large-scale integration (VLSI). Area-time models are further studied in Ref. (Thompson 1980), and the following CMOS cost function is proposed in this reference:

$$Cost_{Area-Delay} = A \times d^P;\ 0 \le P \le 2 \tag{6}$$

where A represents the area of the circuit and d is the delay of the circuit.

The main parameters for computing the function of

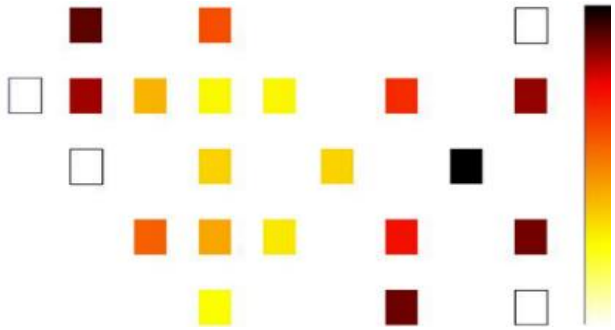


Fig. 7 The dissipation thermal map of the proposed optimized MUX-based SRAM bit cell design in QCA (at 2 K) with 0.5 Ek

Table 3 Energy dissipation of the proposed optimized MUX-based SRAM bit cell

Mode	0.5 E_k	1 E_k	1.5 E_k
Average leakage energy dissipation (meV)	6.01	21.07	36.84
Average switching energy dissipation (meV)	4.38	3.38	2.70
Total energy consumption (meV)	10.39	24.45	39.54

QCA cost are the number of QCA gates and crossovers of the QCA wires, as well as the delay of all zones. Majority gates eliminate irreversible energy, while crossovers cause structural problems and design complexity. Moreover, area and delays affect the performance of the system (Heydari *et al*. 2019). The proposed QCA cost function is given in Eq. (7):

$$Cost_{QCA} = [(M_3 + (F \times M_5))^K + I + C^L] \times (A \times d^P);1 \le K, L, P \tag{7}$$

where the aggregate of 3-input majority gates is shown with a parameter of M_3 and the number of 5-input majority gates is shown with a parameter of M_5, the ratio of the 5-input majority cells number to the aggregate of 3-input majority gate cells is shown with a parameter of F (Khosroshahy *et al*. 2017), the number of inverters is shown with a parameter of I, the number of crossovers is shown with a parameter of C, A represents the area of the QCA circuit, and d is the delay of the circuit (in terms of the number of clock phases). In addition, K is the exponential weightings of the majority gates, while L and P are, respectively, the number of crossovers and delays, which are equal to '2' according to Ref. (Liu *et al*. 2014). Inverters have effect merely on the complexity of QCA circuits, so a constant weight of '1' is considered for them. Moreover, the cost functions use K, L, and P, which affect QCA designs. Prioritizing cost functions requires different criteria depending on the weights of K, L, and P (Liu *et al*. 2014).

The proposed extremely-optimized 2:1 multiplexer has one inverter gate, three three-input majority gates, no crossover, an area of 0.0096 μm^2, and two clock phase delays. Thus, the QCA cost, $Cost_{QCA}$, of the proposed 2:1 multiplexer is equal to 0.384 and the area-delay cost, $Cost_{Area\text{-}Delay}$, is equal to 0.0384. Moreover, the proposed

extremely-optimized MUX-based SRAM bit cell has one five-input majority gate (with F=0.89), three three-input majority gates, one inverter gate, no crossover, an area of 0.0174 μm^2, and four clock phase delay. The value of $Cost_{QCA}$ for the proposed extremely-optimized MUX-based SRAM bit cell is equal to 4.49, and the corresponding $Cost_{Area\text{-}Delay}$ is equal to 0.278.

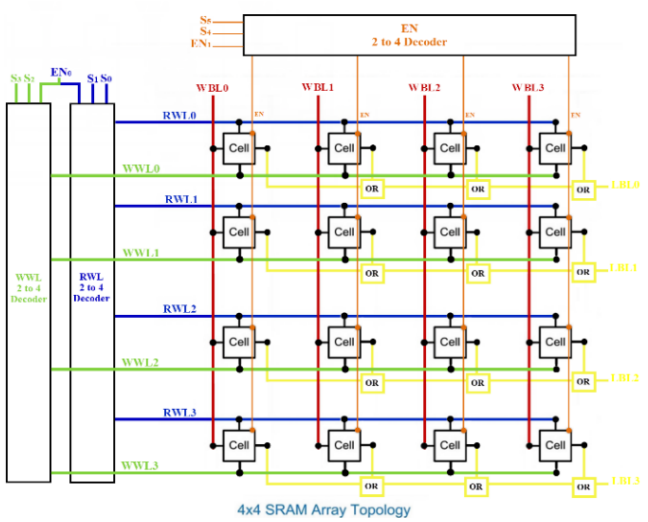
4. Proposed efficient SRAM array in QCA

4.1 4-bit SRAM array in QCA

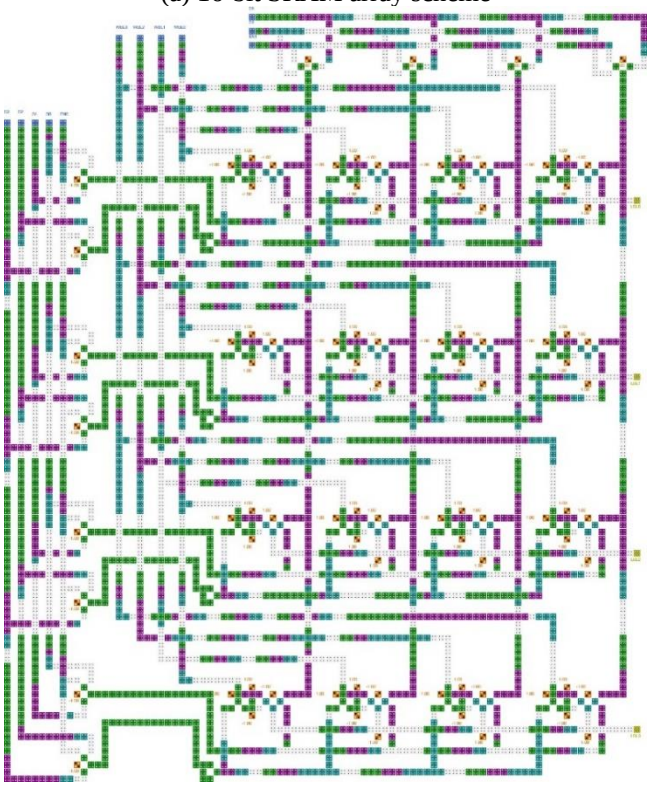
In this section, an efficient 4-bit SRAM array is proposed with a coplanar-free single-layer structure using an optimal SDN at crossovers (Graunke *et al.* 2005, Tougaw and Khatun 2013). The memory array consists of four SRAM cells positioned in a row. A 2-to-4 decoder is used to select individual SRAM cells using the EN cell line, which can be accessed by each cell. The control lines are Read Word Line (RWL) and Write Word Line (WWL). In addition, the Write Bit Line (WBL) inserts data into any selected SRAM cell. The proposed 4-bit SRAM array and the QCA layout are shown in Figs. 8 (a)-(b). This design uses 601 cells, occupies 0.56 μm^2, and requires five clock cycles (20 clock zones). In this QCA-based design, all design rules in terms of layout and timing (Liu *et al.* 2011, Liu *et al.* 2010) have been applied to achieve an optimal design in QCA. In the decoder, if EN = 1 and S1= S0 = 00, the cell on the left of the 4-bit SRAM array is activated. Read or Write operation depends on the value of RWL, WWL, and WBL at this time. In the proposed 4-bit SRAM array, the read and write paths are separate. Therefore, if WWL = 1, the write operation is performed in the cell WBL provides the data. If RWL = 1, a read operation from the cell selected by decoder is performed. The data is then transferred from the output of the SRAM cell to the OR gate and finally to the LBL output because no other data is imported from the inactive SRAM cells.

4.2 16-bit QCA-based SRAM array

SRAM cells are placed in 16-bit arrays (Fig. 9a). A 16-bit SRAM array has four WWL, four RWL, four WBL, and four EN lines, which can address up to sixteen SRAM cells for write and read operations. In the proposed 16-bit SRAM array, WWL 2-to-4 decoder is used to address WWL, WRL 2-to-4 decoder is used to address WRL, and EN 2-to-4 decoder is used to address EN lines. After selecting the desired SRAM cell, one bit of data can be written or read using WWL, RWL, WBL, and EN lines. Write or read operation to/from each of the 16-bit SRAM arrays can be performed separately. In a read operation from SRAM arrays, the data is transferred to the LBLs through OR gates. The layout of the proposed 16-bit SRAM array in QCA is illustrated in Fig. 9(b). This structure is coplanar-free single-layer and uses optimal SDN (Abedi *et al.* 2015) at crossovers (i.e., clocking-based coplanar crossover). The proposed 16-bit SRAM array in QCA contains 3485 cells covering an area of 3.97 μm^2. The implemented 16-bit



(a) 16-bit SRAM array scheme



(b) 16-bit SRAM array layout in QCA

Fig. 9 The proposed 16-bit SRAM in QCA

SRAM array in QCA has a maximum delay of eight clock cycles (32 clock zones).

4.3 n×m-bit SRAM array in QCA

A module with a fixed structure and a correct timer can be built with a 16-bit SRAM provided in the previous section. We can merge two or four modules that can produce 32-bit or 64-bit QCA SRAM arrays using appropriate connections. Using these arrays, one can expand the SRAM lines and create n×32-bit or n×64-bit SRAM memories. The width of SRAM can also be increased depending on memory usage.

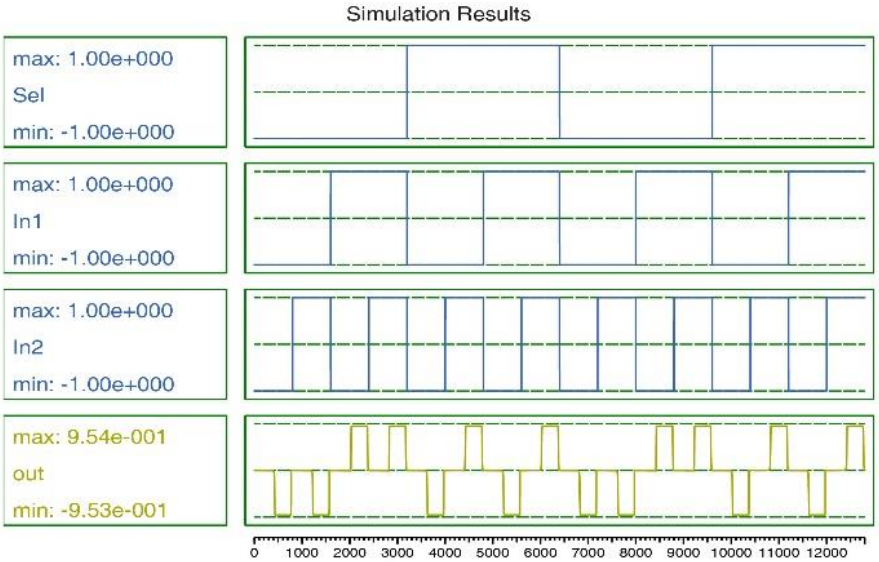


Fig. 10 Simulation of the suggested extremely-optimized 2:1 multiplexer in QCA

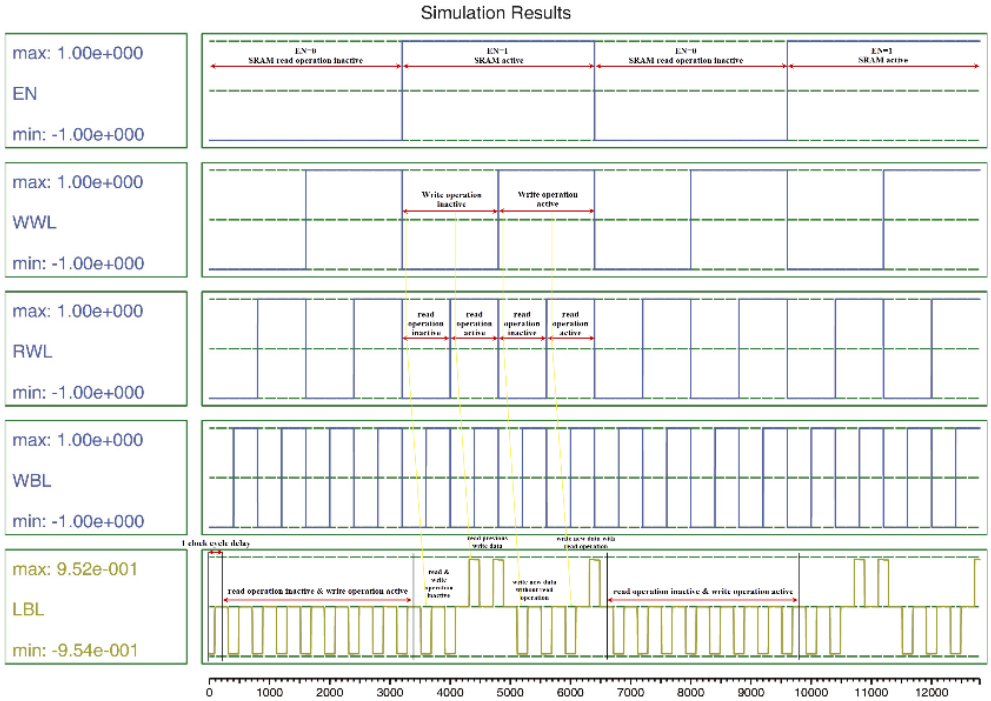


Fig. 11 Simulation results of the extremely-optimized MUX-based SRAM bit cell in QCA

5. Simulation results and comparisons

The proposed QCA SRAM bit cell circuit is simulated employing QCADesigner 2.0.3 (Walus *et al*. 2004). All adjustable values of QCADesigner are set as default.

Fig. 10 illustrates the results of simulation of the extremely-optimized 2:1 multiplexer in QCA. These results prove the proper performance of the multiplexer. In this figure, all modes are precisely occurring; the output is included in In1 and In2 when Sel values '0' and '1', respectively.

Fig. 11 depicts the results of the simulation of the QCA-based SRAM cell. These results validate the proper performance of the proposed designs. For example, in a write operation with EN=1, WWL=1, and RWL=0 or 1, after one clock cycle delay, the new input data reaches the output. In addition, during a read operation with EN=1, WWL=0, and RWL=1, the old data is locked inside the loop regardless of the input data value. Besides, if EN = 0, the SRAM cell is inactive during the read operation.

The results of the 2-to-4 decoder simulation are presented in Fig. 12. These results prove the appropriate performance of the proposed 2-to-4 decoder. As illustrated in Fig. 12, all modes precisely occur; outputs are enabled (disabled) when EN is active (inactive).

The performance parameters of the 2:1 multiplexer are

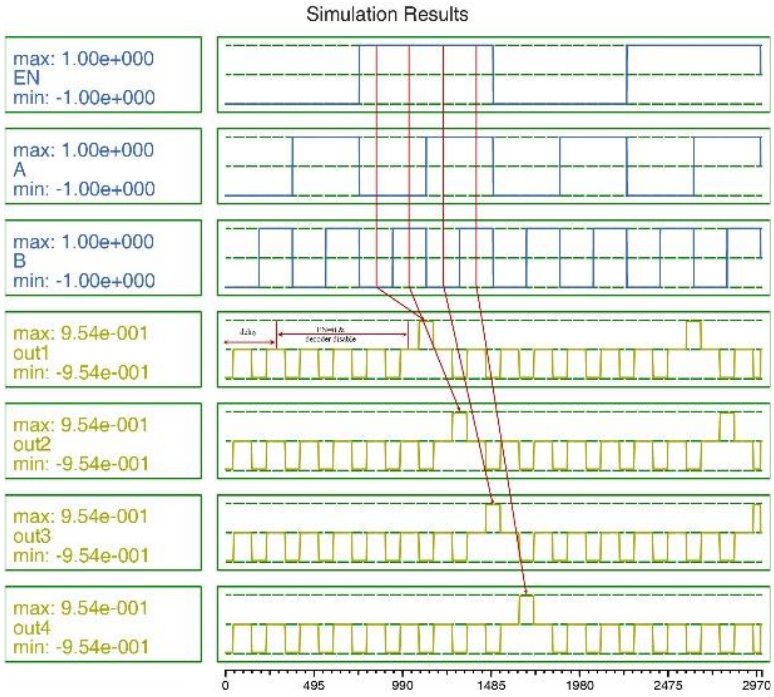


Fig. 12 Simulation of the suggested 2-to-4 decoder in QCA

Table 4 Comparison of the suggested extremely-optimized 2:1 multiplexer with previous designs

	Area (μm^2)	Complexity (#cells)	delay (clock cycles)	Cost$_{QCA}$ function (FOM)	Cost$_{Area\text{-}Delay}$ function (FOM)
Proposed 2 to 1 multiplexer – (18nm)	0.0096	13	0.5×10^{-12}s	0.384	0.0384
QCA 2 to 1 multiplexer of (Ahmad 2017) – (18nm)	0.01	16	0.5×10^{-12}s	0.4	0.04
QCA 2 to 1 multiplexer of (Das and De 2016a) – (18nm)	0.016	21	0.75×10^{-12}s	1.44	0.144
QCA 2 to 1 multiplexer of (Das and De 2016b) – (18nm)	0.012	17	0.5×10^{-12}s	0.48	0.048
QCA 2 to 1 multiplexer of (Sabbaghi-Nadooshan and Kianpour 2014) – (18nm)	0.016	26	0.5×10^{-12}s	0.64	0.064

Table 5 Comparison of the energy consumption of the suggested extremely-optimized 2:1 multiplexer with previous designs

	Average leakage energy diaaiplation (*meV*)			Average switching energy diaaiplation (*meV*)			Total energy consumption (*meV* ($\times10^{-3}$*eV*))		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Proposed 2 to 1 multiplexer – (18nm)	3.59	10.28	17.87	6.03	4.89	3.16	9.62	15.17	21.03
QCA 2 to 1 multiplexer of (Ahmad 2017) – (18nm)	6.19	15.56	25.54	7.79	6.26	4.98	13.98	21.82	30.52
QCA 2 to 1 multiplexer of (Das and De 2016a) – (18nm)	5.5	17.38	31.17	26.83	22.66	18.91	32.33	40.04	50.08
QCA 2 to 1 multiplexer of (Das and De 2016b) – (18nm)	4.54	13.88	24.63	11.41	9.77	8.19	15.95	23.65	32.82
QCA 2 to 1 multiplexer of (Sabbaghi-Nadooshan and Kianpour 2014) – (18nm)	6.79	21.16	38.27	35.22	30.37	25.85	42.01	51.53	64.12

presented in Table 4. The results show that the suggested extremely-optimized 2:1 multiplexer has a smaller area, fewer cells, lower delay, and less QCA cost than the best previous designs (Ahmad 2017, Das and De 2016a, b, Sabbaghi-Nadooshan and Kianpour 2014). Moreover, the dissipation of the proposed 2:1 multiplexer is compared with previous designs in Table 5 (Ahmad 2017, Das and De 2016a, b, Sabbaghi-Nadooshan and Kianpour 2014).

Table 6 is presented the efficiency parameters of QCA memory cells. The results show that the suggested

Table 6 Comparison of the suggested extremely-optimized MUX-based SRAM bit cell with previous designs

	Area (μm^2)	Complexity (#cells)	delay (clock cycles)	$Cost_{QCA}$ function (FOM)	$Cost_{Area-Delay}$ function (FOM)
Proposed SRAM bit cell – (18nm)	0.0174	22	1×10^{-12}s	4.49	0.278
QCA memory cell of (Song *et al*. 2020) – (18nm)	0.026	26	1×10^{-12}s	7.49	0.416
QCA memory cell of (Kianpour and Sabbaghi-Nadooshan 2016) – (18nm)	0.05	52	1.5×10^{-12}s	34.20	1.8
QCA memory cell of (Khosroshahy *et al*. 2017) – (18nm)	0.06	71	1.25×10^{-12}s	50.46	1.5
QCA memory cell of (Angizi *et al*. 2015) – (18nm)	0.08	88	1.5×10^{-12}s	169.20	2.88
QCA memory cell of (Hashemi and Navi 2012) – (18nm)	0.13	109	1.75×10^{-12}s	242.06	6.37
CMOS SRAM cell (Shin *et al*. 2011) – (22nm)	0.0741	6-Transistor	$\approx\times10^{-9}$s	-	-
FinFET SRAM cell (Oh *et al*. 2017) – (22nm)	0.17	9-Transistor	$\approx\times10^{-9}$s	-	-
FinFET SRAM cell (Karl *et al*. 2016) – (14nm)	0.05	6-Transistor	$\approx\times10^{-9}$s	-	-

Table 7 Comparison of the energy consumption of the suggested extremely-optimized MUX-based SRAM bit cell with previous designs

	Average leakage energy diaaiplation (*meV*)			Average switching energy diaaiplation (*meV*)			Total energy consumption (*meV* ($\times10^{-3}$*eV*))		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Suggested SRAM bit cell	6.01	21.07	36.84	4.38	3.38	2.70	10.39 / 1.66	24.45 / 3.91	39.54 / 6.33
QCA memory cell of (Song *et al*. 2020)– (18nm)	7.65	21.51	37.23	20.39	17.31	14.61	28.04 / 4.49	38.82 / 6.21	51.84 / 8.29
QCA memory cell of (Kianpour and Sabbaghi-Nadooshan 2016)– (18nm)	20.91	59.43	103.02	60.93	52.01	43.85	81.84 / 13.09	111.44 / 17.83	146.87 / 23.50
QCA memory cell of (Khosroshahy *et al*. 2017) – (18nm)	25.20	70.04	120.09	72.51	61.13	51.26	97.71 / 15.63	131.17 / 20.99	171.35 / 27.42
QCA memory cell of (Angizi *et al*. 2015) – (18nm)	26.23	78.83	140.48	128.78	112.44	96.80	155.01 / 24.80	191.27 / 30.60	237.28 / 37.97
QCA memory cell of (Hashemi and Navi 2012)– (18nm)	30.39	95.78	174.25	164.69	143.33	122.26	195.08 / 31.21	239.11 / 38.26	296.51 / 47.44
FinFET SRAM cell (Oh *et al*. 2017) – (22nm)	-	-	-	-	-	-	average energy: 3.72 (MeV ($\times10^3$eV)) / 0.595 (pJ ($\times10^{-12}$J))		
FinFET SRAM cell (Yang *et al*. 2014)– (22nm)	-	-	-	-	-	-	average energy: 16.875 (MeV ($\times10^3$eV)) / 2.7 (pJ ($\times10^{-12}$J))		

extremely-optimized MUX-based SRAM bit cell occupies a smaller area, requires fewer cells, as well as having lower delay, and less QCA costs than the best structures in the literature (Hashemi and Navi 2012, Angizi *et al*. 2015, Khosroshahy *et al*. 2017, Kianpour and Sabbaghi-Nadooshan 2016, Song *et al*. 2020). Moreover, the comparison of the proposed extremely-optimized MUX-based SRAM bit cell in 18 nm QCA and the SRAM bit cell in 22 nm CMOS, and in 22 and 14 nm FinFET technologies are presented in Table 5 (Shin *et al*. 2011, Oh *et al*. 2017 and Karl *et al*. 2016). Based on the results in Table 6, the proposed extremely-optimized MUX-based SRAM bit cell is superior to previous designs from different aspects, such as area occupation, cell count, delay, and QCA cost (Hashemi and Navi 2012, Angizi *et al*. 2015, Khosroshahy *et al*. 2017, Kianpour and Sabbaghi-Nadooshan 2016, Song *et al*. 2020, Shin *et al*. 2011, Oh *et al*. 2017, Karl *et al*. 2016).

The energy analysis of the SRAM bit cells in QCA is illustrated in Table 7 for three different E_k (0.5, 1, and 1.5 E_k) at 2 degrees kelvin. According to these results, the extremely-optimized MUX-based SRAM bit cell has lower energy consumption than the best previous structures. The results demonstrate that the proposed optimized MUX-based SRAM bit cell has improved the energy consumption compared to the designs previously presented in the literature (Hashemi and Navi 2012, Angizi *et al*. 2015, Khosroshahy *et al*. 2017, Kianpour and Sabbaghi-Nadooshan 2016, Song *et al*. 2020, Oh *et al*. 2017, Yang *et al*. 2014).

Overall, the comprehensive results of simulation designate that the proposed extremely-optimized MUX-based SRAM bit cell has a smaller area, fewer cells, lower delay, less QCA cost, and lower SRAM bit cell energy consumption compared to previously designed QCA memories (Hashemi and Navi 2012, Angizi *et al*. 2015,

Table 8 Comparison of the suggested 4-bit SRAM array with previous designs

	Area (μm^2)	Complexity (#cells)	delay (clock cycles)	$Cost_{QCA}$ function (FOM)	$Cost_{Area-Delay}$ function (FOM)
Proposed array – (18nm)	0.56	601	5×10^{-12}s	115103.81	224
QCA memory array of (Song *et al*. 2020) – (18nm)	0.79	704	5×10^{-12}s	221075.16	316
QCA memory array of (Mubarakali *et al*. 2019) – (18nm)	1.09	843	6×10^{-12}s	481239.36	627.84
QCA memory array of (Heydari *et al*. 2019) – (18nm)	1.16	860	5.75×10^{-12}s	491525.64	613.64

Khosroshahy *et al*. 2017, Kianpour and Sabbaghi-Nadooshan 2016 and Song *et al*. 2020) and SRAMs in MOSFET and FinFET technologies (Shin *et al*. 2011, Oh *et al*. 2017, Karl *et al*. 2016, Yang *et al*. 2014). These promising improvements are of great importance in the field of digital systems.

Table 8 compares the delay, cost, area, and complexity of the proposed 4-bit SRAM array and some other designs reviewed in the present study (Song *et al*. 2020, Mubarakali *et al*. 2019, Heydari *et al*. 2019). The results show the superiority of the proposed structure, which uses only one layer without crossovers.

6. Conclusions

In the present study, an extremely-optimized 2:1 multiplexer and an extremely-optimized MUX-based SRAM bit cell were proposed in QCA. The proposed designs used the loop-based SRAM approach with higher energy efficiency, smaller area, less complexity, lower delay, and lower QCA cost. Additionally, expandability and better management were realized by properly placing the input and output cells in the suggested design. The new SRAM cell structure has direct read capability. This paper also presented 4-bit and 16-bit SRAM array designs in QCA technology. The presented SRAM arrays showed high efficiency, as well as low area occupation, complexity, delay, QCA cost, and energy dissipation in QCA integrated circuits. Moreover, QCADesigner and QCApro were used as simulation tools and their results showed the advantages of the proposed QCA structures over previous ones in terms of energy dissipation, complexity, QCA cost, delay, and area.

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