Advances in Nano Research, *Vol. 10, No. 1 (2021) 91-99*
DOI: https://doi.org/10.12989/anr.2021.10.1.091

Device modelling and performance analysis of two-dimensional $AlSi_3$ ballistic nanotransistor

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(*Received July 21, 2020, Revised November 10, 2020, Accepted November 20, 2020*)

Abstract. Silicene is an emerging two-dimensional (2D) semiconductor material which has been envisaged to be compatible with conventional silicon technology. This paper presents a theoretical study of uniformly doped silicene with aluminium ($AlSi_3$) Field-Effect Transistor (FET) along with the benchmark of device performance metrics with other 2D materials. The simulations are carried out by employing nearest neighbour tight-binding approach and top-of-the-barrier ballistic nanotransistor model. Further investigations on the effects of the operating temperature and oxide thickness to the device performance metrics of $AlSi_3$ FET are also discussed. The simulation results demonstrate that the proposed $AlSi_3$ FET can achieve on-to-off current ratio up to the order of seven and subthreshold swing of 67.6 mV/dec within the ballistic performance limit at room temperature. The simulation results of $AlSi_3$ FET are benchmarked with FETs based on other competitive 2D materials such as silicene, graphene, phosphorene and molybdenum disulphide.

Keywords: doped silicene; ballistic transport; 2D material; I-V characteristics; nanotransistor

1. Introduction

Two-dimensional (2D) materials for nanoelectronic applications are rigorously under research as the semiconductor industry is entering the post-Moore's Law era, within a decade (Chhowalla *et al*. 2016, Chuan *et al*. 2019). Moreover, the ultra-thin body (or nanosheet) transistor is foreseen as the last resort for transistor scaling (Ye *et al*. 2019). The recent advances in 2D materials are driven by the success of graphene (Novoselov *et al*. 2005, Ghannadpour and Moradi 2019, Shariati *et al*. 2020), giving rise to exploration and research interests in various 2D materials such as phosphorene (Goswami and Gawande 2019), hexagonal boron nitride (Lim *et al*. 2018), transition metal dichalcogenides (Radisavljevic *et al*. 2011), and silicene (Zhao *et al*. 2016). In addition, silicene is selected as one of the potential emerging materials for device miniaturisation in the International Roadmap for Devices and Systems (IRDS) (Badaroglu 2018).

Silicene is a monolayer of silicon (Si) atoms arranged in graphene-like lattice structure. Density Functional Theory (DFT) calculations have theoretically predicted the possibility of silicene in the 1990s (Takeda and Shiraishi 1994). Similar to graphene, silicene exhibits ultra-high carrier mobility due to the Dirac cones property at the *K*-point in its electronic band structure (Vogt *et al*. 2012, Sun *et al*. 2016). Although the fabrication of free-standing silicene is still in its infancy stage (Sarebanha *et al*. 2017), silicene has been experimentally formed on various surfaces (Sadeddine *et al*. 2017, Hsu *et al*. 2018, Stępniak-Dybala and Krawiec 2019, Si and Niu 2020). One of the most successful techniques to grow 2D group IV material such as silicene is the molecular beam epitaxial growth (Izhnin *et al*. 2020, Si and Niu 2020). In 2015, the first silicene Field-Effect Transistor (FET) was fabricated and characterised by employing synthesis-transfer fabrication process (Tao *et al*. 2015). Tao *et al*. (2015) showed that the experimentally measured intrinsic mobility of their silicene device (~100 $cm^2\ V^{-1}s^{-1}$) is much lower than theoretically predicted intrinsic mobility of free-standing silicene (~1000 $cm^2\ V^{-1}s^{-1}$) possibly due to the substrate effects on silicene. However, this is a stepping stone for future research and development featuring silicene.

2. Related research

Unlike the gapless pristine graphene (Wong *et al*. 2019), pristine silicene has an extremely small energy band gap of 1.55 meV when the spin-orbit effect is included (Liu *et al*. 2011). Nevertheless, this extremely small energy band gap is still hindering the applications of pristine silicene in the future nanoelectronic logic circuits, which typically requires an energy band gap of at least 0.4 *eV* (Ni *et al*. 2014). To overcome this major drawback, previous studies on uniformly doped silicene with aluminium (Al), denoted as $AlSi_3$ hereafter, revealed that this band gap engineering technique has effectively opened the band gap to a value that is suitable for switching applications (Ding and Wang 2013, Chuan *et al*. 2020a). Although single- and multiple-doping techniques are able to induce band gaps in silicene, the electronic properties of the single- or multiple-doped monolayer silicene are strongly dependent on the locations

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ISSN: 2287-237X (Print), 2287-2388 (Online)

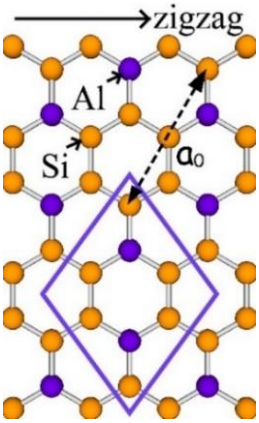


Fig. 1 Schematic diagram of 2D $AlSi_3$ lattice structure where a_0 is the lattice constant. The brown and blue atoms represent silicon (Si) and aluminium (Al) atoms, respectively. The primitive unit cell is enclosed in blue parallelogram

of the dopants (Chen *et al*. 2014). Thus, uniform doping technique is chosen in the present work.

Salimian and Dideban (2019) investigated the silicene nanoribbon (SiNR) FET by using transfer matrix method and reported an on-to-off current (I_{on}/I_{off}) ratio up to the order of seven. Besides, Lima *et al*. (2018) presented I_{on}/I_{off} ratio as high as 10^6 for silicene-based FET using *ab-initio* ballistic transport simulation. Despite various published silicene-based transistor models such as Patel and Choudhary (2017), Lima *et al*. (2018), Salimian and Dideban (2019), Chuan *et al*. (2020b), minimal effort has been directed to assess the potential application of uniformly doped silicene as a FET. Therefore, this work is proposed to examine the device performance of $AlSi_3$ FET.

In this paper, the electronic properties of $AlSi_3$ in the zigzag (ZZ) direction as shown in Fig. 1, is computed by employing Nearest Neighbour Tight-Binding (NNTB) approach described in Chuan *et al*. (2020a) and the parabolic band assumption using the method described in Chuan *et al*. (2020c). By employing this method, the electronic transport properties of the carriers in $AlSi_3$ can simply be described by the transverse effective masses which are later applicable in the top-of-the-barrier (ToB) ballistic transistor model as described in Section 3.2. The ToB ballistic transistor model is simple and widely used to predict the performance limits of new materials for FET applications (Chuan *et al*. 2020d). In Section 4, the simulation results of $AlSi_3$ are shown by plotting the behaviour of electrons at the ToB and current-voltage (I-V) characteristics. Moreover, the extracted device performance metrics of $AlSi_3$ FET are benchmarked with other 2D materials. Finally in Section 5, the conclusion of this study is drawn.

3. Theoretical modelling

The modelling procedures and equations used for the electronic properties of $AlSi_3$ and I-V characteristics of $AlSi_3$ FET are described in details in this section.

Table 1 Parameters of NNTB model for $AlSi_3$

a_0 (Å)	t_{Al-Si} (eV)	t_{Si-Si} (eV)	E_{0Si} (eV)	E_{0Al} (eV)
8.11	−1.05	−1.02	−7.59	−5.71

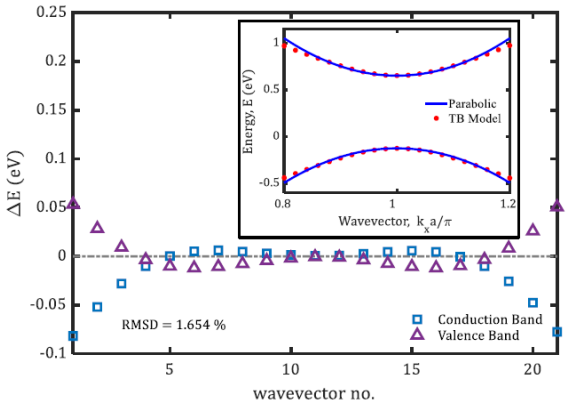


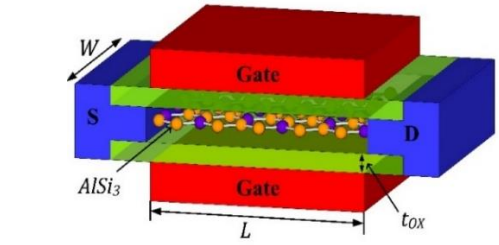
Fig. 2 Plot of RMSD for the effective mass approximation. Inset: The parabolic band structure

3.1 Electronic properties of $AlSi_3$

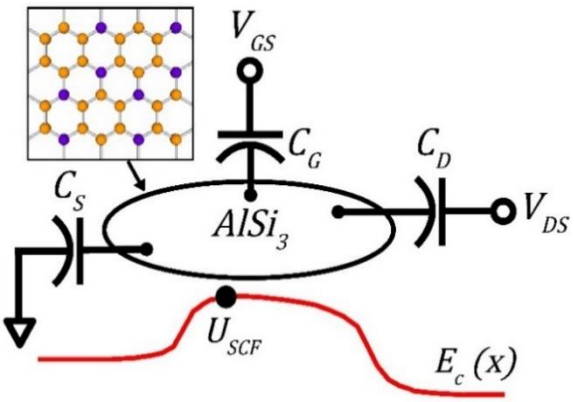
The atomic structure of 2D $AlSi_3$ is shown in Fig. 1. Unlike pristine silicene which is stable in the buckled lattice structure (Ding and Ni 2009), the published DFT calculations by Ding and Wang (2013) found that the monolayer $AlSi_3$ is stable in its planar structure. The electronic band structure of $AlSi_3$ in the ZZ direction is modelled using the NNTB approach. In this work, the honeycomb lattice structure of $AlSi_3$ is assumed to have perfect 120° internal hexagonal angles. By fitting the DFT calculations from Ding and Wang (2013), the parameters for the NNTB are obtained. The computed parameters for NNTB are shown in Table 1 where a_0 is the lattice constant (Ding and Wang 2013), $t_{Al-Si} = t_{Si-Al}$ is the hopping integral for Al-Si (or Si-Al) bonds (Chuan *et al*. 2020a) and t_{Si-Si} is the hopping integral for Si-Si bonds, E_{oSi} and E_{oAl} are the on-site energies for Si and Al atoms (Harrison 2004), respectively.

The effective masses for the electrons and holes at the conduction band and valence band are extracted using the parabolic band equations (Arora 2015, Chuan *et al*. 2020c). The calculated band gap of $AlSi_3$ of the present model is 0.78 *eV*, which is between the DFT-PBE gap and DFT-HSE gap (Ding and Wang 2013). Despite the band gap differences, all the band structures show consistent p-type doping descriptions for $AlSi_3$ nanosheet. The extracted effective masses in the ZZ direction are $m_e^* = 0.235m_0$ for electron and $m_h^* = 0.255m_0$ for holes, where m_0 is the constant for electron rest mass. The parabolic band fitting procedure is evaluated by using the normalised Root-Mean-Square-Deviations (RMSD) (Kazmierski *et al*. 2009, Leong *et al*. 2020), which is given by

$$RMSD = \frac{\sqrt{\sum_{i=1}^{N}(p_i - q_i)^2/N}}{\max(p_i, q_i) - \min(p_i, q_i)} \times 100\% \qquad (1)$$



(a) Structural model



(b) Circuit model

Fig. 3 Model of $AlSi_3$ FET where t_{OX} is the oxide thickness; C_D, C_S and C_G are the drain, source, and gate capacitances, respectively; V_{GS} and V_{DS} are gate and drain voltage, respectively; $E_c(x)$ is the conduction band and U_{SCF} is self-consistent potential at the ToB

where N denotes the total number of data, p_i and q_i are the values of i^{th} data for the NNTB model and parabolic band model, respectively.

Fig. 2 shows the plot for RMSD calculations. The energy differences, ΔE clearly show that the model fits best at the minimum point of conduction band and the maximum point of the valence band. By applying Eq. (1), the normalised RMSD for the parabolic band fitting procedure is 1.654%, indicating that the parabolic band model has fitted the NNTB model accurately at the conduction band and valence band with minimal errors. From the inset in Fig. 2, it is observed that valence band of $AlSi_3$ is closer to the Fermi energy level E_F (set at 0 *eV* in this work), verifying the p-type doping properties because Al is a trivalent element. Subsequently, the proposed $AlSi_3$ FET focuses on the current flow via the conduction band where the performance of the FET depends primarily on the electron mobility (Md Arshad *et al*. 2015).

3.2 Transistor model

The double-gated $AlSi_3$ FET device model as shown in Fig. 3(a) is simulated in this paper where W is the width, L is the channel length and t_{OX} is the oxide thickness. The gate oxide used for the $AlSi_3$ FET is SiO_2 (with a dielectric constant of ε_r = 3.9) with t_{OX} = 1.5 nm and gate length is 10 nm. Monolayer $AlSi_3$ in the ZZ direction is used as the conducting channel between the source and drain terminals. Ballistic transport (L « mean free path) and ideal terminal contacts are assumed.

The circuit model of the ToB ballistic transistor (Rahman *et al*. 2003) consists of the gate capacitor (C_G), source capacitor (C_S), and drain capacitor (C_D) as depicted in Fig. 3(b). In this work, the source is grounded at V_S = 0 *V* for all bias points. Voltage is applied at two terminals, namely drain and gate. The drain voltage V_{DS} lowers the Fermi level in the drain, draining the electrons from the channel that are injected from the source. On the other hand, the positive gate voltage V_{GS} lowers the potential energy barrier at the ToB in the $AlSi_3$ channel. The self-consistent potential is placed at the ToB to determine the mobile charge. The model does not include the calculation of quantum capacitance explicitly. However, the effect of quantum capacitance is treated within the self-consistent gate electrostatics calculations (Rahman *et al*. 2003).

In order to obtain the electron concentrations at the ToB, the density of states and Fermi-Dirac distribution equations are required. The DOS (Supriyo 2017) for the $AlSi_3$ with length L and width W is obtained as

$$D(E) = g\frac{m_e{}^* LW}{2\pi\hbar^2}\vartheta(E - E_C) \tag{2}$$

where g is the degeneracy factor (2 is used to include up and down spins), $\vartheta(E - E_C)$ is the Heaviside unit step function (Thriveni and Ghosh 2019), $\hbar = h/2\pi$ is the Planck's constant, and $m_e{}^*$ is the electron effective mass obtained in Section 3.1. Fermi-Dirac distribution (Lundstrom and Jeong 2013) which describes the occupancy probability of a state at a given temperature T, is given as

$$f(E) = [1 + \exp(\frac{E - E_F}{k_B T})]^{-1} \tag{3}$$

where k_B =1.38 × 10^{-23} J/K is the Boltzmann constant.

The modelling procedure starts by computing the equilibrium electron concentration, N_0 at the ToB by using

$$N_0 = \int_{-\infty}^{+\infty} D(E) f_0(E)\ dE \tag{4}$$

where $D(E)$ is the DOS as shown in Eq. (2) and $f_0(E)$ is the Fermi-Dirac distribution at equilibrium. After that, the induced mobile charge contributed by the source and drain terminals is computed at each specific applied V_{GS} and V_{DS}, described by

$$N_S = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_S(E_S)\ dE \tag{5a}$$

and

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_D(E_D)\ dE \tag{5b}$$

where the source and drain Fermi functions are defined as

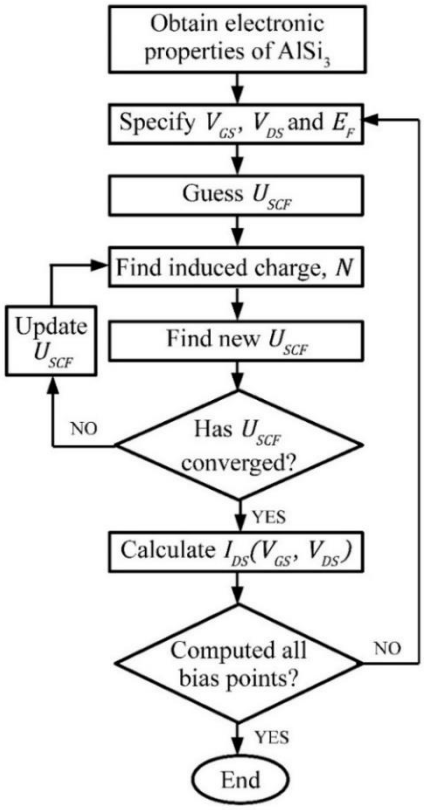


Fig. 4 Flow chart of self-consistent calculation to compute the I-V characteristics for the transistor model (Supriyo 2017)

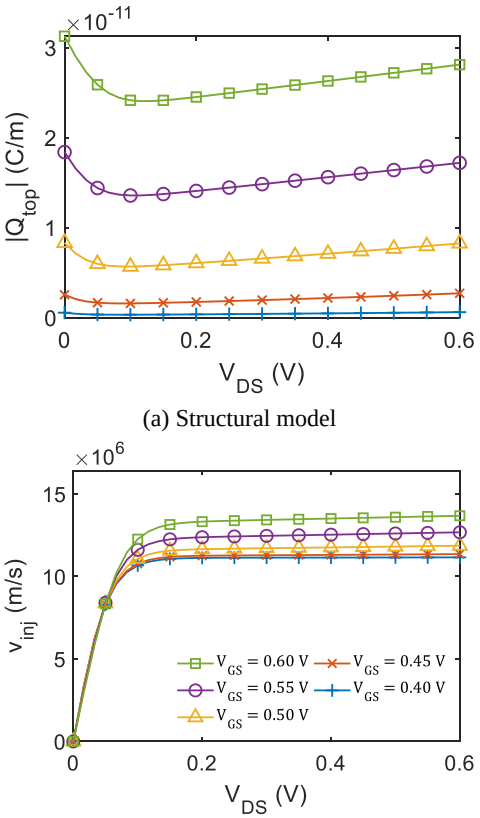


Fig. 5 (a) Electron charge Q_{top}; (b) average electron injection velocity v_{inj} at the ToB (both at T = 300K) as a function of drain voltage V_{DS}. The legend for (a) is the same as in (b)

$f_S(E_S) \equiv f(E + U_{SCF})$ and $f_D(E_D) \equiv f(E + U_{SCF} + qV_{DS})$, respectively. When voltage is applied at the drain, a non-equilibrium condition is created, where the positive velocity states are filled by the source and the negative velocity states are filled by the drain. The net mobile charge at the ToB is then obtained as $\Delta N = (N_S + N_D) - N_0$.

The self-consistent potential at the ToB, U_{SCF} is obtained by using the superposition between the Laplace potential (without the presence of mobile charge), $U_L = -q(\alpha_G V_{GS} + \alpha_D V_{DS} + \alpha_S V_S)$ and potential that floats up, $U_P = q^2 \Delta N / C_\Sigma$ due to the net mobile charge ΔN. The complete equation of the self-consistent potential at the ToB is obtained as

$$U_{SCF} = U_L + U_P = -q\left(\alpha_G V_{GS} + \alpha_D V_{DS} + \alpha_S V_S - q\frac{\Delta N}{C_\Sigma}\right) \quad (6)$$

where q is the electric charge constant and $C_\Sigma = C_G + C_D + C_S$ is the parallel combination of terminal capacitances. $\alpha_G = C_G/C_\Sigma$, $\alpha_D = C_D/C_\Sigma$, $\alpha_S = C_S/C_\Sigma$ are the capacitive coupling factors for gate, drain, and source, respectively. In this paper, the default parameters, α_G = 0.880 and α_D = 0.035 (Rahman *et al*. 2003) are considered. Since $V_S = 0$ *V* for all bias points, α_S can be ignored.

Eqs. (5) and (6) are solved self-consistently to obtain N and U_{SCF} for each specific bias point. Finally the drain current is evaluated by using the Landauer-Büttiker ballistic transport equation (Supriyo 2017), expressed as

$$I_{DS}(V_{GS}, V_{DS}) = \frac{q}{h}\int_{-\infty}^{+\infty} M(E)[f_S(E_S) - f_D(E_D)]\,dE \quad (7)$$

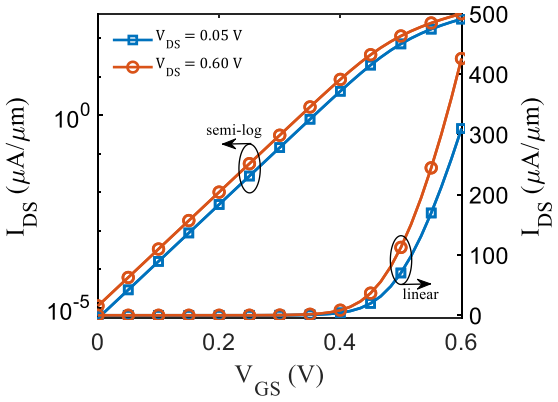
where

$$M(E) = g\frac{2W}{h}\sqrt{2m_e^*(E - E_c)}\,\vartheta(E - E_C) \quad (8)$$

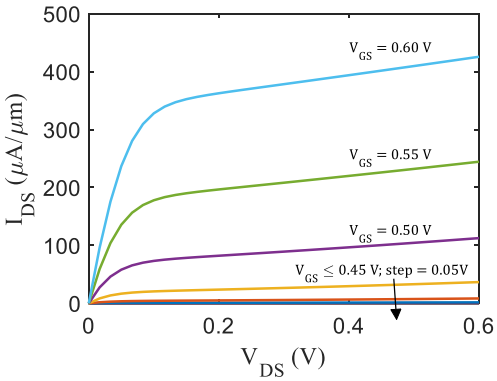
is the number of modes. Fig. 4 depicts systematically the self-consistent iterative computational procedures (Chuan *et al*. 2020d). The magnitude of the supply voltage in this work is 0.6 *V* and the E_F is adjusted such that the off-current is I_{off} = 10^{-5} μA/μm. This ballistic current transport equation is widely employed because the conventional scattering-limited mobility of carriers can no longer accurately describe the I-V characteristics of nanoscale FETs, where the electric field becomes extremely strong in the channel (Saad *et al*. 2009).

4. Results and discussions

This section shows the simulation results of $AlSi_3$ FET



(a) $I_{DS} - V_{GS}$ characteristics



(b) $I_{DS} - V_{DS}$ characteristics

Fig. 6 I-V characteristics of $AlSi_3$ FET

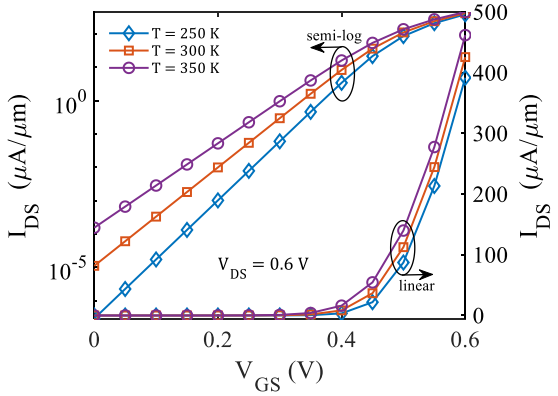


Fig. 7 Transfer $(I_{DS} - V_{GS})$ characteristics of $AlSi_3$ FET at T = 250K, T = 300K (room temperature) and T = 350K at V_{DS} = 0.6 V

and the comparative benchmark with other published results.

4.1 Charge and velocity

Prior to plotting the I-V characteristics, the carrier behaviour at the ToB is examined analytically. The charge density and the carrier injection velocity at the ToB are calculated using

$$\left|Q_{top}(V_{GS}, V_{DS})\right| = \left|-q[N_S(V_{GS}, V_{DS}) + N_D(V_{GS}, V_{DS})]\right| \quad (9)$$

and

$$\langle v_{inj}(V_{GS}, V_{DS})\rangle = \frac{I_{DS}(V_{GS}, V_{DS})}{\left|Q_{top}(V_{GS}, V_{DS})\right|} \quad (10)$$

respectively. Note that both quantities are calculated as a function of V_{GS} and V_{DS}, as described in Section 3.2.

Figs. 5(a) and (b) depict the charge and injection velocity at the ToB, respectively. It is observed that the charge at the ToB is nearly independent of V_{DS} at the degenerate regime. However, the initial dip of the curve could be improved by using the floating source method (Rahman *et al*. 2003). Moreover, the injection velocities saturate as V_{DS} has been increased to the degenerate regime (above approximately 0.2 *V*). The saturated injection velocities v_{inj} under ballistic transport are 1.2 × 10^7 m/s at V_{GS} = 0.4 *V*, 1.3 × 10^7 m/s at V_{GS} = 0.5 *V* and 1.5 × 10^7 m/s at V_{GS} = 0.6 *V*. This saturation of velocity can be used to explain the current saturation in the I-V characteristics at the saturation regime. Although the carriers are under ballistic transport, that is, transport without any scattering mechanism, the drain current saturation can still occur when V_{DS} is greater than a few k_BT/q, due to the thermal injection velocity limit (Lundstrom and Antoniadis 2014).

4.2 Current-voltage characteristics

The I-V characteristics are initially computed for $AlSi_3$ FET at room temperature, T = 300K. The transfer $(I_{DS} - V_{GS})$ characteristics are plotted in Fig. 6(a) and the output $(I_{DS} - V_{DS})$ characteristics are plotted in Fig. 6(b). By maintaining the same device structure, the I-V characteristics are computed for different operating temperature as shown in Fig. 7. This is done to examine the performance of $AlSi_3$ FET transistor at a lower (T = 250K) and higher (T = 350K) operating temperatures. Moreover, simulations are also done to obtained the I-V characteristics of $AlSi_3$ FET at a thinner (t_{OX} = 0.5 nm) and a thicker (t_{OX} = 3.0 nm) gate oxides at room temperature, T = 300K as plotted in Fig. 8.

4.3 Device performance and analysis

Table 2 shows the device performance of $AlSi_3$ FET at various temperature and performance benchmark with various 2D FET models (where all the 2D FET are modelled using the ToB ballistic transistor model for fair comparison). The device performance metrics extracted for $AlSi_3$ FET are based on the graphical method as shown in Fig. 9.

The simulation results for $AlSi_3$ FET at various temperatures (as shown in Fig. 7) show that the device performance could degrade at a higher temperature. At higher temperature, the SS and DIBL are increased while I_{on}/I_{off} ratio is decreased. From Fig. 7, it is clearly observed that high temperature increases the I_{off} but I_{on} is not much affected by the temperature, causing the I_{on}/I_{off} ratio to decrease. The degraded performance due to high temperature could cause undesired switching error (due to the threshold voltage shift) and higher static power

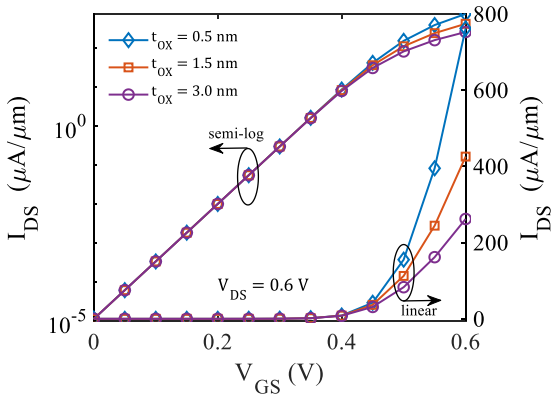


Fig. 8 Transfer ($I_{DS} - V_{GS}$) characteristics of $AlSi_3$ FET with difference oxide thicknesses at T = 300K (room temperature) and V_{DS} = 0.6 V

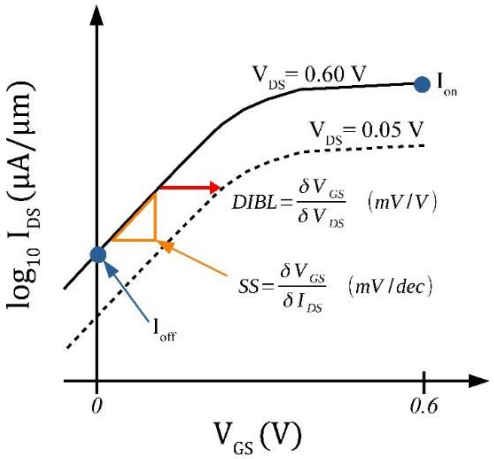


Fig. 9 Extraction and definitions of device performance metrics from the transfer characteristics of a FET (Wong *et al*. 2020)

consumption (due to higher I_{off}) when the FET is applied in digital logic nanoelectronic circuits. This shows that efficient heat dissipation is essential for a nanoelectronic circuit to operate in a stable manner (Wang *et al*. 2019). On the other hand, one interesting characteristic can be observed in Fig. 7, where the saturation of current is almost independent on temperature. This could be due to the unique characteristic of ballistic transport where the carrier velocity is independent of temperature at the degenerate regime of the semiconductor, which is shown in previous studies (Ahmadi *et al*. 2008, Lim *et al*. 2018, Chuan *et al*. 2020d).

Fig. 8 examines the effect of oxide thickness t_{OX} to the device performance of $AlSi_3$ FET. It is clearly shown that I_{on}/I_{off} ratio decreases when the t_{OX} for SiO_2 increases. This decrease in I_{on}/I_{off} ratio is due to the decrease in on-current, where this observation is more clearly shown in the linear scale plot in Fig. 8. However, the extracted device performance metrics show that the thickness of SiO_2 has no effects on the off-current, SS and DIBL. This observation is due to the limitation of the present model where this model has considered the Laplace potential (U_L) by using the linear combinations of $-q(\alpha_G V_{GS})$ and $-q(\alpha_D V_{DS})$ with α_G and α_D as the adjustment parameters to match SS and DIBL. In this work, fitting constants are used for α_G and α_D as shown in Section 3.2. These assumptions are overestimating the effects of gate electrostatic control at the subthreshold regime. Thus, in future work, the gate electrostatic control could be improved by using the solution of Poisson equation. Moreover, the gate tunnelling current could also be taken into account to improve the investigation on the effects of t_{OX} to the performance of the FET (Dong and Guo 2017, Lu *et al*. 2017).

The device performance metrics for $AlSi_3$ FET are benchmarked with a few published results on other 2D FETs, namely Graphene Nanoribbon (GNR) (Eshkalak *et al*. 2015), phosphorene (Lam *et al*. 2014), MoS_2 (Hosseini and Karami 2018), and SiNR (Poljak 2020). In this case, the comparison is only done for the operating temperature of T = 300K due to the limitation of available data from the published results. Surprisingly, $AlSi_3$ FET outperforms GNR FET (Eshkalak *et al*. 2015), phosphorene FET (Lam *et al*. 2014) and SiNR FET (Poljak 2020). However, the performance of $AlSi_3$ FET is slightly lower than MoS_2 FET (Hosseini and Karami 2018). This could be due to the high-k dielectric used in the MoS_2 FET model. Nevertheless, this slight drawback can be compensated by the fact that silicene has the potential to be compatible with the present

Table 2 Performance benchmark for $AlSi_3$ FET model with published 2D FET results

Ref.	Device parameters (refer to Fig. 3(a))				Device metrics		
	Channel material	t_{OX} (nm)	L (nm)	T (K)	SS (mv/dec)	DIBL (mv/V)	I_{on}/I_{off} ratio
This work	$AlSi_3$	0.5	10.0	300	67.7	48.1	6.8×10^7
This work	$AlSi_3$	1.5	10.0	250	56.4	44.39	1.3×10^9
This work	$AlSi_3$	1.5	10.0	300	67.7	48.1	3.8×10^7
This work	$AlSi_3$	1.5	10.0	350	79.0	53.0	3.0×10^6
Eshkalak *et al*. (2015)	GNR	1.5	10.0	300	83.9	51.1	4.5×10^4
This work	$AlSi_3$	3.0	10.0	300	67.7	48.1	2.4×10^7
Lam *et al*. (2014)	Phosphorene	3.0	20.0	300	-	-	1.0×10^4
Hosseini and Karami (2018)	MoS_2	3.0	10.0	300	67.0	-	4.7×10^7
Poljak (2020)	SiNR	1.0	15.0	300	60.0	25.0	2.8×10^6

fabrication process which is heavily depending on Si (Tao *et al*. 2015). In addition, silicene is very attractive as the knowledge on the Si-based devices is mature in the semiconductor industry.

5. Conclusions

The FET with uniformly doped silicene, namely $AlSi_3$ as the conducting channel is modelled and simulated in this paper. The effective mass of $AlSi_3$ in the ZZ direction is obtained by fitting the parabolic band structure to the NNTB band structure. ToB ballistic transistor model is employed to compute the I-V characteristics. The device performance metrics and performance analysis of $AlSi_3$ FET are also presented. In addition, the effects of temperature to the device performance of $AlSi_3$ FET are discussed. The theoretical results of $AlSi_3$ FET show comparable device performance after benchmarking with other 2D FETs, namely GNR FET, phosphorene FET, MoS_2 FET and SiNR FET. However, modelling procedures for gate electrostatic control should be improved to better predict the SS and DIBL. In addition, more information on the device performance can be obtained by incorporating non-ballistic transport effects such as elastic scattering, tunnelling effect, and phonon scattering into the existing model for further insights.

Acknowledgments

The authors acknowledge the Research Management Centre (RMC) of Universiti Teknologi Malaysia (UTM) for providing excellent support and a stimulating research environment. Mu Wen would like to convey his gratitude for the award of PhD Zamalah Scholarship from the School of Graduate Studies, UTM. Michael Tan would like to acknowledge the financial support from UTM Fundamental Research (UTMFR) Grant (Vote no.: Q.J130000. 2551.21H51), which allowed the smooth progress of this research.

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