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Design of non-volatile digital circuit with assuming magnetic tunneling junction and carbon nanotubes field-effect transistors devices

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Abstract. Power consumption has become the key constraint in electronics design, since the MOSFET threshold and hence the supply voltage can no longer be scaled. This trend calls for new device concepts such as Spintronic devices that are fundamentally different from CMOS. A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. Magnetic tunnel junction (MTJ) is an emerging technology which has many advantages when used in logic in memory structures in conjunction with CMOS. In this paper, we present novel designs of hybrid CNTFET-MTJ circuits; AND, XOR and 1-bit full adder. The proposed CNTFET-MTJ full adder design has 20 times lower Power-delay-product (PDP) compared to the previous CMOS- MTJ full adder. Also, the delay in CNTFET-MTJ circuit is reduced 20 times compared to the CMOS- MTJ circuit.

Keywords: Magnetic Tunnel Junction (MTJ); Carbon Nanotube Field-Effect Transistor (CNTFET); low power circuit; non-volatile digital circuit; spintronics

1. Introduction

Spintronic is the use of electron spin instead of its charge in processing and transmitting data. Spin of the electrons in bound quantum nano-structures have a long phase relaxation time and a considerable phase coherence length. Based on this, components such as spin memories, spin transformers, and spin filters have been designed and manufactured. Spintronic chips are equivalent to microelectronic chips that work with less energy, more power, and more speed. This technology was developed in 2007 with the half-metallic ferromagnetic growth (Chappert *et al*. 2010, Lu *et al*. 2020) and. The first element was the Spin Torque Transfer Magnetic Tunnel Junction (SST-MTJ), which was used to design non-volatile memories. Based on the structure of the same element, other elements have also been presented that are now mostly in design and simulation mode (Kim *et al*. 2015a). The main attraction of spintronic elements for logical applications is due to their non-volatile nature, which can provide computational systems with zero static power and the possibility of instantaneous and immediate on-off switch. CNTFET transistors, as a new and promising generation of transistors, are able to overcome most of the basic limitations of MOSFETs. A ballistic or quasi-ballistic transfer can be achieved by an intrinsic carbon nanotube, under low-voltage bias to achieve unlimited element performance. Designing digital circuits with the special capabilities of CNTFET transistors and combining them with non-volatile MTJ elements can create new advantages and challenges in this combination. In this study, we want to examine the design process of basic CNTFET-MTJ binary-based gates.

Sharifi and Thapliyal (2017) has provided a comprehensive design of CMOS-MTJ hybrid circuits for the implementation of digital binary control. Which is a good comparison with the FINFET-MTJ combination. The most important parameters considered in this article are latency power consumption and power–delay product (PDP). The technology used in simulation is CMOS22nm.

Adiabatic CMOS-MTJ and Non-Adiabatic CMOS-MTJ circuits have been also provided. In Adiabatic circuits, the capacitor is charged using a constant-current source, unlike Non-Adiabatic circuits, which is done with a constant voltage source. Due to this technique, the power consumption of the circuit is reduced (Sharifi *et al*. 2017, Taheri *et al*. 2020).

Solving the Reliability problem of a sensing amplifier (SA) with high sensing margin for the CMOS-MTJ Combined Logic Circuit has been studied in many articles. Using a gate designed in CMOS 40 nm technology, a compressed MTJ model, CMOS/MTJ combination circuit and Mont Carlo statistical simulation, the performance and efficiency of this sensing amplifier have been evaluated (Zhang *et al*. 2017a).

Good ideas for designing, continuing and building CMOS-MTJ circuits have been examined. In fact, the future of CMOS-MTJ circuits with layout design is one of the main challenges of new research (Hanyu *et al*. 2016).

Another important challenge for circuits that use MTJ as

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a non-volatile element is the PCSA circuit. A reliability-enhanced separated pre-charge sensing amplifier (RESPCSA) has been provided for CMOS-MTJ combinational logic circuits (Zhang *et al*. 2017b).

The circuit optimization technique has been provided for LUT circuits is based on the logic of non-volatile memory and has MTJ elements, the output latency, power and area of the circuit have been evaluated. Estimates show that the MTJ element has affected the performance of these circuits (Suzuki *et al*. 2019).

Non-volatile memory based on the combination of SRAM and STT-MTJ cells to reduce energy consumption includes a lot of research. An NV-SRAM compound cell can have a special application for the Internet of Things. (Prasad *et al*. 2019).

The reduction in reading-writing error rate in MTJ has been investigated by adding a loop circuit to CMOS-MTJ circuits using the MTJ model with three terminals, which has led to a reduction in power loss (Onizawa *et al*. 2018).

Solving the problem of power leakage using the advantages of non-volatile circuit is another challenge of CMOS-MTJ hybrid circuits. Solving this problem will lead to the design of future generation microprocessors (Rajaei and Mamaghani 2017).

In some references, all collectors have been designed with no power loss gating capability. These circuits store all inputs in the MTJ using the spin-transfer torque (STT) method and with the help of the spin-hall effect (SHE). Power consumption and MTJ switching latency have been significantly reduced by using SHE (Amirany and Rajaei 2018, Abualnour *et al*. 2019, Belbachir *et al*. 2019, Medani *et al*. 2019).

Chaabane *et al*. (2019) presented static and dynamic behaviors of functionally graded beams (FGB) is presented using a hyperbolic shear deformation theory. Boulefrakh *et al*. (2019) presented a simple quasi 3D hyperbolic shear deformation model for bending and dynamic behavior of functionally graded (FG) plates resting on visco-Pasternak foundations. Karami *et al*. (2019) studied size-dependent wave propagation analysis of functionally graded (FG) anisotropic nanoplates based on a nonlocal strain gradient refined plate model. Boukhlif *et al*. (2019) studied a dynamic investigation of functionally graded (FG) plates resting on elastic foundation using a simple quasi-3D higher shear deformation theory. Addou *et al*. (2019) investigated the effect of Winkler/Pasternak/Kerr foundation and porosity on dynamic behavior of FG plates using a simple quasi-3D hyperbolic theory. Semmah *et al*. (2019) investigated the thermal buckling characteristics of zigzag single-walled boron nitride (SWBNNT) embedded in a one-parameter elastic medium. Mahmoudi *et al*. (2019) applied a refined quasi-three-dimensional shear deformation theory for thermo-mechanical analysis of functionally graded sandwich plates. Kaddari *et al*. (2020) studied structural behaviour of functionally graded porous plates on elastic foundation using a new quasi-3D model.

This article has been organized in the following sections: The first section examined the introduction and review of the research conducted, and in the second section, the structure of the elements used in circuit design is examined. Section 3 presented the proposed design of CNTFET-MTJ combinational circuits. In this section, digital base circuits are designed using the proposed combination. Finally, the simulation results are discussed and compared with similar studies in the fourth and fifth sections.

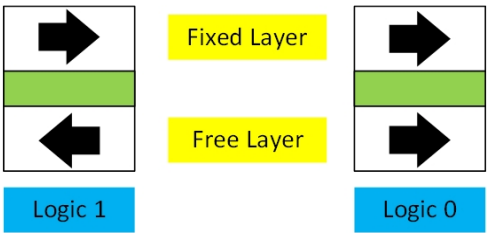

Fig. 1 Representation of logic 0 and 1 in MTJ

2. Structure of elements

A - MTJ structure

In the MTJ element, the magnetic orientation of one ferromagnetic layer is fixed and the direction of the other layer (by applying a polarized spin current through the element) (free layer) can be changed. When the spins are aligned, there is lower resistance and when they are not aligned, there is higher resistance. Therefore, the high resistance is attributed to logic 1 and the lower resistance is attributed to logic 0, which remains unchanged for the magnetization of the free layer by shutting the applied field off. Therefore, it is used to store single-bit data in memory (Flatte 2007).

Since an MTJ is a memory element, there are two processes in it. 1- The process of recording the logical mode in MTJ and controlling the free layer momentum and in other words its switching, which is known as “writing” in MTJ; 2- The process of sensing this state recorded in MTJ and getting a logical output from it, which is known as “reading” from MTJ.

Therefore, after writing, the electrical resistance of the MTJ must be measured by circuits to design logical outputs. This resistance is measured by a Sensing amplifier. An MTJ can be simply modeled as a variable resistor. If the free layer is connected to terminal (A)+ and the fixed layer is connected to terminal (B)-, the current will be established from A to B, which is shown in Fig. 2.

An MTJ can be assumed to be in one of two states of parallel (low) and anti-parallel (high) resistance and representation of hysteresis behavior. The resistance hysteresis curve shown in Fig. 3, as shown, the change in resistance is a function of the voltage or current applied to the MTJ.

A positive voltage or current (V_{MTJ}/i_{MTJ}) switches the MTJ from high to low resistance and vice versa. But by applying voltage + when MTJ is in parallel (P) state or voltage - when it is in anti-parallel (AP) state, there is no change in MTJ state and the element remains in the same state. The current or voltage at which the switch and change

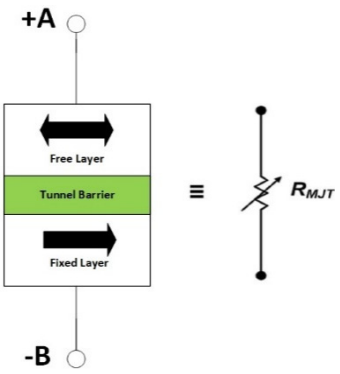

Fig. 2 MTJ model with resistance

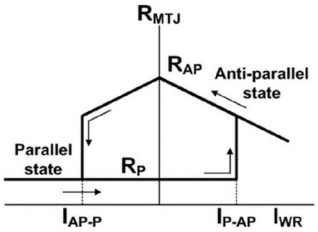

Fig. 3 Hysteresis curve of MTJ resistance

occurs has been called the critical current (threshold) (Ic); depending on the states, the critical current or voltage + and - (Ic+/Vc+, Ic-/Vc-) has been defined.

Therefore, the TMR[1] ratio is defined as follows

$$TMR = \frac{R_{AP} - R_P}{R_P} \quad (1)$$

Considering the effect of tunnel magneto resistance (TMR), the change in resistance depends on the relative level of the free and fixed layers in the MTJs.

B - CNTFET transistor

Fig. 4 presents the structure of a CNTFET that, its main difference is the use of CNTs instead of the CMOS semiconductor channel.

After scaling the integrated circuit made of silicon, their physical limitation to change to nanoscale is one of the major challenges. Thus, CNTFET will become popular in the range of integration technology of the next generation. This is due to its superior specifications such as semiconductor nanotubes, which have created high mobility, ballistic transmission and nano dimensions are other features. Single-layer or multi-layer graphenes form a nanotube with a bee-like lattice arrangement that resembles a cylindrical shape. Carbon nanotubes can be semi-conductor or metallic, which depends on the piping orientation, which is known as the carial phenomenon. Therefore, this structure leads to the creation of a transistor with the sub-threshold switch voltage and creates excellent performance in the nanoelectric field. Because of the I-V

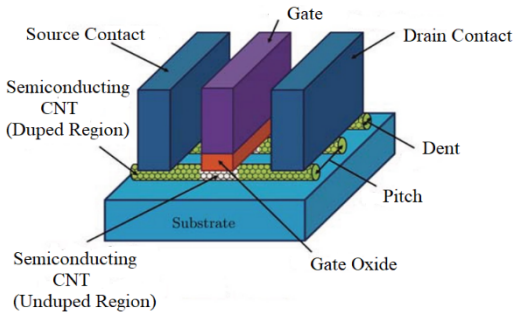

Fig. 4 An example of a CNTFET structure

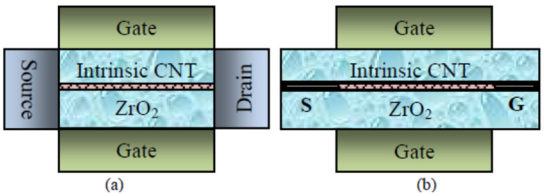

Fig. 5 Two types of CNTFET: (a) Schottky barrier CNTFET (SB); (b) MOSFET-like CNTFET

characteristics in CNTFET compared to the same characteristics in MOSFET, scientists have been encouraged to replace MOSFET with CNTFET in many applications.

CNTFETs have different types depending on the structure of the gate and the channel. As shown in Fig. 5, there are basically two types of CNTFET, named CNTFET, similar to MOSFET and SB-CNTFET. The CNTFET channel, similar to MOSFET, consists of an intrinsic semiconductor CNT. This transistor depends in function on the height-barrier modulation theory. Where the channel has been composed of the intrinsic semiconductor SB-CNTFET CNT, direct tunneling is applied through the Schottky barrier (SB) at the source-channel junction in the semiconductor nanotubes. The transmitting conductivity of this SB-CNTFET is controlled by the gate voltage, which is modeled according to the width-barrier by gate voltage.

The research uses the MOSFET-like CNTFET transistor structure, modeled in Vijayan *et al*. (2018). The Hspice code of the same model has been also used in the simulation.

3. Proposed design-combined structure of CNTFET-MTJ in digital circuit

The CNTFET-MTJ combinational circuit follows the block structure of Fig. 6. There are three main blocks in this figure. The energy storage element, or memory element is MTJ or an element based on the structure of spintronic elements. The CNTFET transistor realizes the logic of switching digital circuits, in fact coupling between memory and output elements is done using the CNTFET transistor. The PCSA sensing amplifier determines the level of logic at

[1] Tunnel magneto resistance

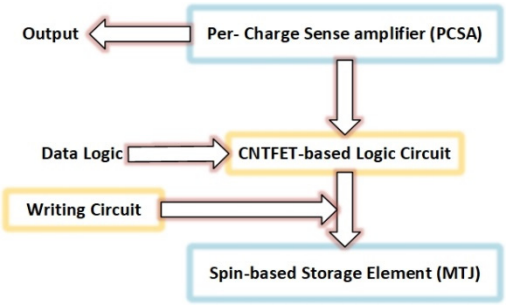

Fig. 6 Diagram block of CNTFET-MTJ combinational structure

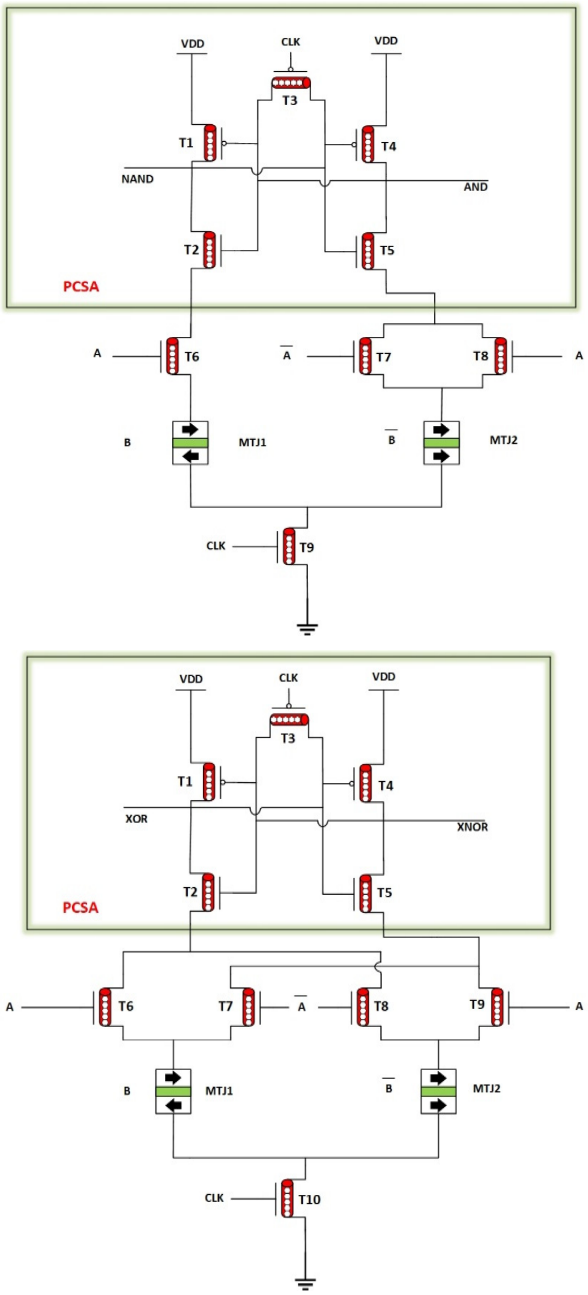

Fig. 7 The proposed XOR and AND gates with the combined structure of CNTFET-MTJ, where the initial states of MTJ1 and MTJ2 are anti-parallel and parallel, respectively

the output, which is also built using CNTFET performance. The sensing amplifier circuit is of the pre-charge type, which we will explain in the next section according to the type of circuit. The important point of all circuits of this research is that all transistors are of CNTFET type.

A) CNTFET-MTJ combinational circuits

This section has proposed the basic logic and arithmetic gates (AND, XOR, and Full Adder circuit) using the CNTFET-MTJ combinational structure. The proposed design uses a simple sensing amplifier compared to existing models.

3.1 Design of AND and XOR gates

The schematic presentation of the architecture proposed by AND and XOR gates can be seen in Fig. 7. This schematic is based on dynamic logic. In the pre-charge phase (CLK = 0), the transistor T3 is on and the output voltage reaches the voltage $V_{DD} - V_{th}$. In the evaluated phase (CLK = 1), T3 is off and T9 is on, therefore, the outputs are determined according to the input pattern. For example, in the XOR circuit, when B = 1 and A = 0, the MTJ1 and MTJ2 states are parallel and anti-parallel, respectively. With this input pattern, T7 and T8 are on as a result, due to the lower resistance of MTJ1, they are discharged to the earth faster. The significant point is that the initial states of MTJ1 and MTJ2 are parallel and anti-parallel, respectively.

Unlike conventional logic and arithmetic circuits, they used two PCNTFETs to pre-charge the output at a voltage of V_{DD}; in this design, a PCNTFET has been used in the pull up network to pre-charge the outputs. Fig. 8 shows the AND gate with the combined structure of CNTFET-MTJ. In the proposed circuits, in the evaluation phase, one of the

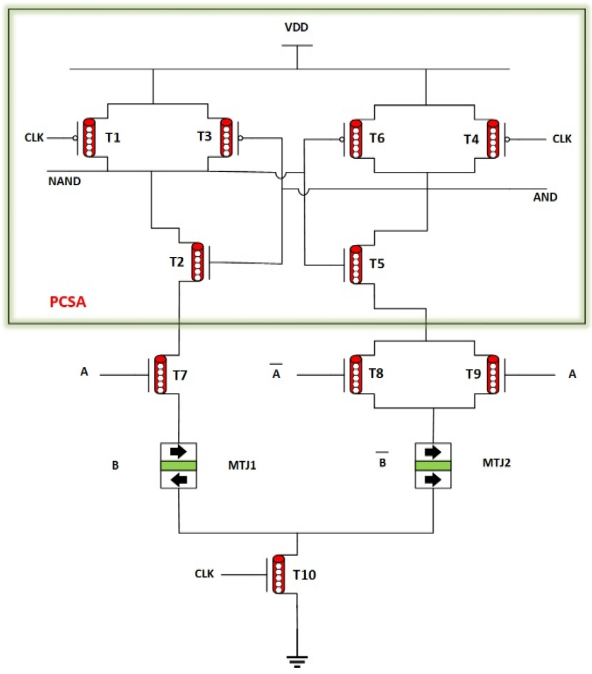

Fig. 8 AND gate, with combined CNTFET-MTJ structure

outputs is discharged to the earth and the other is charged at the voltage of V_{DD}.

In the next phase, when the CLK is zero, we will have a voltage sharing at the output nodes as a result, it is less costly than previous designs. Also, in the pre-charge phase, the outputs are not fully charged to the voltage of V_{DD}. Compared to existing designs, we need less time and therefore less latency to discharge the outputs.

3.2 Full Adder design

The schematic design of the Full Adder cell has been described in Fig. 9. The performance of this circuit is similar to the XOR and AND gates, the Sum and $Cout$ output functions can be observed in Eqs. (2) and (3).

$$sum = A \cdot B \cdot C_{in} + A \cdot \bar{B} \cdot \overline{C_{in}} + \bar{A} \cdot \bar{B} \cdot C_{in} + \bar{A} \cdot B \cdot \overline{C_{in}} \quad (2)$$

$$Cout = A \cdot B + A \cdot C_{in} + B \cdot C_{in} \quad (3)$$

The following is a description of a Full Adder cell. Considering the inputs B = 1, MTJ1 and MTJ2 are parallel and anti-parallel, respectively. If A = 1 and $Cin = 1$, the output Sum is discharged faster through T2, T6, T8 and MTJ1. In the case where the input pattern for $ABCin$ is 011, Sum output will be discharged to earth via T5, T11, T19 and MTJ1. For other input patterns, the outputs are determined according to Eqs. (1) and (2). The transient response of the hybrid CNTFET-MTJ is shown in Fig. 10, and it confirms the correct operation of the proposed full adder cell.

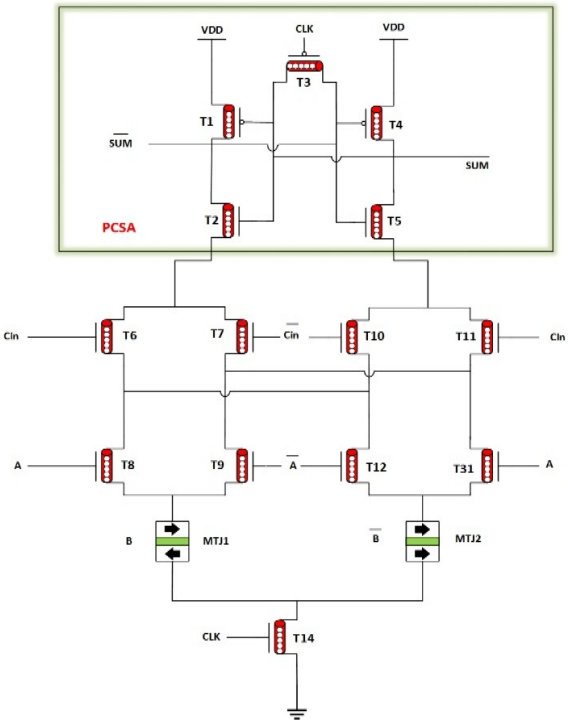

Fig. 9 The full adder circuit, with the combined structure of CNTFET-MTJ, where the initial states of MTJ1 and MTJ2, are anti- parallel and parallel, respectively

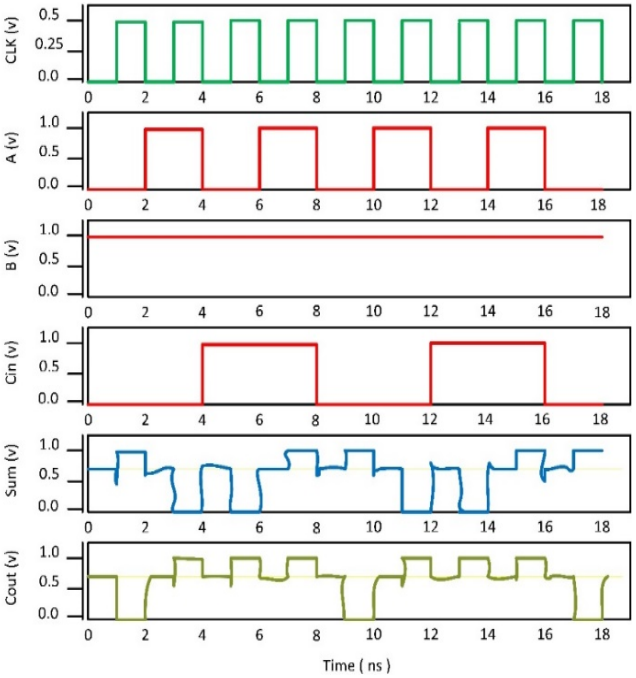

Fig. 10 Transient response of the proposed hybrid CNTFET-MTJ full adder circuit

3.3 Theoretical analysis of energy consumption in the proposed CNTFET-MTJ circuit

This section theoretically analyzes the energy consumption in the proposed CNTFET-MTJ circuit. For analysis, let us consider the CNTFET-MTJ AND gate (see Fig. 7). Generally, the energy dissipated to charge a capacitor is given by

$$E_{diss} = \frac{1}{2} C V_{dd}^2 \quad (4)$$

Where C is the load capacitance value and V_{dd} is the voltage swing.

V_{dd} during the previous cycle. During the charge sharing phase of the proposed CNTFET-MTJ AND gate, output voltages will be pre-charged to $V_{dd} - V_{th}$. During this phase, both the nodes have $V_{dd} - V_{th}$ (AND and NAND). So, the total energy dissipated in the charge sharing phase of the proposed CNTFET-MTJ XOR gate is given by

$$E_{diss,charge-sharing} = \frac{1}{2} C (V_{dd} - V_{th})^2 + \frac{1}{2} C (V_{th})^2 \quad (5)$$

Similarly, during the evaluate phase of the CLK, one of the two outputs (AND or NAND) will be discharged to ground, while the other output will be charged to V_{dd}. So, the energy dissipated during the evaluate phase of the CLK is given by

$$E_{diss,eval} = \frac{1}{2} C (V_{dd} - V_{th})^2 + \frac{1}{2} C (V_{th})^2 \quad (6)$$

So, the total energy dissipated in one clock cycle of the existing CNTFET-MTJ AND gate is given by

$$E_{diss,CNTFET-MTJ} = E_{diss,charge-sharing} + E_{diss,eval} \quad (7)$$

$$E_{diss,CNTFET-MTJ} = C(V_{dd} - V_{th})^2 + C(V_{th})^2 \quad (8)$$

Now we want to have a numerical comparison between the energy dissipated in the provided circuit and the CNTFET-MTJ circuit. For example, let us consider C = 0.8 fF, VDD = 1 V, and Vth = 0.21V. From Eq. (8), the energy dissipated for the proposed CNTFET-MTJ circuits is 0.5345 fJ. Theoretically, it is found that reducing the threshold voltage of the CNTFET-MTJ circuit, causes energy dissipated is greatly reduced.

4. Simulation results AND discussion

This section examines the simulation results on the proposed circuit. It is tried to compare the simulation results with the reference circuits, which is structurally similar to the proposed design. For this comparison, we should keep in mind that the MTJ model and the CNTFET transistor odel are identical, or at least similar in terms of parameters. We have used HSPICE software for simulation. MTJ is of CoFeB/MgO type with HSPICE reference model. The CNTFET transistor model has been derived from the Stanford University CNFET Model. Table 1 shows the MTJ parameters, which are used in our simulations.

Table 1 MTJ parameters

Description	Parameters	Value
Thickness of the free layer	t_{sl}	1.3 nm
Length of surface long axis	L	40 nm
Width of surface short axis	W	40 nm
Thickness of the oxide barrier	t_{ox}	0.85
Tunnel magneto resistance ratio	TMR	170%
Resistance area product	R_A	$5\ \Omega\mu m^2$
MTJ layout surface	A	$40\ nm \times 40\ nm \times \pi/4$
Critical switching current	I_{co}	$40\ \mu A$

The simulation results, including the worst case delay, the average power consumption, and the PDP of the designs, are presented in Table 2. We compared our designs with a CMOS current mode circuit (CML) due to its similar circuit structure to the hybrid CMOS-MTJ circuits and an CMOS-MTJ circuit structure. (Vijayan *et al*. 2018) As shown in Table 2, the proposed designs have lower power consumption and consequently lower PDP compared to the state-of-the-art designs (Kim *et al*. 2015b). The proposed CNTFET-MTJ NAND, XOR, and full adder designs have very low PDP, compared to the previous CMOS-MTJ designs. As it is mentioned before, the input B is assumed to be constant "1", but if we toggle this input and include its writing power to the whole power consumption, the PDP improvement of the proposed full adder will be 32%.

5. Conclusions

The CMOS-MTJ combination has been used in all the articles reviewed in this research, which were reviewed in the introduction of the research. But the digital circuit composition based on CNTFET-MTJ has been less studied. The unique nanotechnology properties of CNTFET transistors in digital circuit design have been proven in research to date. CMOS technology has many limitations in designing high-speed switching circuits. Parameters such as circuit energy consumption, speed or latency, and the ability of nanoscale ultra-compact integrations in CNTFET transistors are improving every day. The MTJ element is the key element in the design of non-volatile digital circuits. Research related to this element is out of the concept and the results of research that leads to the laboratory construction of the element are published every day. We were looking for a key combination in this study. The CNTFET-MTJ combination can form one of the best digital hybrid circuits. Therefore, in this research, we have designed digital base circuits such as NAND and XOR gates. Then, we have designed and simulated the entire collector circuit by using these gates. The simulations have

Table 2 Simulation results of the proposed designs compared to the published designs

Type of circuit	Logic circuit	Delay (e-11)	Power (e-6)	PDP (e-17)
Basic CML (Vijayan *et al*. 2018)	NAND	4.360	13.52	39.32
CMOS-MTJ (Rajaei and Mamaghani 2017)		19.69	3.026	41.85
Proposed CNTFET-MTJ		1.362	0.636	1.145
Basic CML (Vijayan *et al*. 2018)	XOR	4.421	15.32	49.18
CMOS-MTJ (Rajaei and Mamaghani 2017)		20.63	3.005	39.62
Proposed CNTFET-MTJ		3.502	0.659	1.836
Basic CML (Vijayan *et al*. 2018)	Full Adder	7.785	21.78	146.3
CMOS-MTJ (Rajaei and Mamaghani 2017)		24.75	4.536	89.18
Proposed CNTFET-MTJ		3.355	1.096	3.052

been performed in HSPICE software environment. The simulation results showed that the energy consumption of the all-collector circuit based on the CNTFET-MTJ combination has been 30 times lower than that of the similar CMOS-MTJ circuit. The latency of switching is 8 times smaller than that of the CMOS-MTJ circuit. Of course, the parameter of latency can be expanded by changing the design process. The accuracy of the operation of the collector circuit is acceptable and the PCSA circuit couples the performed calculations correctly to the output. The circuit designed in this research can be the basis of other digital circuits based on the CNTFET-MTJ combination.

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